SPD1179 Circuit Design Guide

Preface

SPD1179 is the SOC microcontroller launched by Spintrol for automotive applications, which is highly integrated. It is equipped with a 32-bit high-performance ARMCortex-M4F core, a software programmable clock frequency of up to 100MHz, 32KB SRAM, 128KB embedded FLASH, 1KB EEPROM simulated by 12KB FLASH software, and rich enhanced I/O and peripheral resources. In addition, it also provides 13-bit ADC, 1 differential and 1 single-ended programmable gain amplifier, 4 enhanced PWM modules, 3 general-purpose 32-bit timers, 2 UARTs (hardware supports LIN), 2 SPI, 1 I2C and 1 CAN communication interfaces.

SPD1179 adopts a wet-side QFN package with 48 or 56 pins, supporting single power supply of 5.5V~40V, with integrated power management module, supporting sleep mode and stop mode to reduce power consumption, integrating cascade charge pump and current-type three-phase pre-driver, also integrating LIN transceiver, supporting working temperature of -40 ~ +150 ℃. It can drive brushed and brushless motors, with advantages of high integration, high reliability and low device cost.

SPD1179 is an ideal platform for motor control applications in the field of automotive electronics, and has been widely used in control of car windows, sunroofs, seats, electric sliding doors, wipers, rearview mirrors, tailgates, laser radar, oil pumps, water pumps, thermal management, air conditioning compressors, blowers, electronic fans, flaps, etc. This document focuses on the problems often encountered in circuit design of SPD1179, and recommends some practical circuits.

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Revision history

Revision	Date	Author	Status	Changes
C/0	2024-04-11	DL.Gong, S.Xu	Outdated	First release.
C/1	2024-07-24	MC.Rao	Released	1. Modify section 1.3.1 notice that writing a Word in EEROM takes 42 microseconds. 2. Add the selection of decoupling capacitor voltage rating for DVDD5 and DVDD5EXT in Table 1-3. 3. Adjust the description in section 1.6. 4. Adjust the impedance and diode characteristics comparison table in section 6.

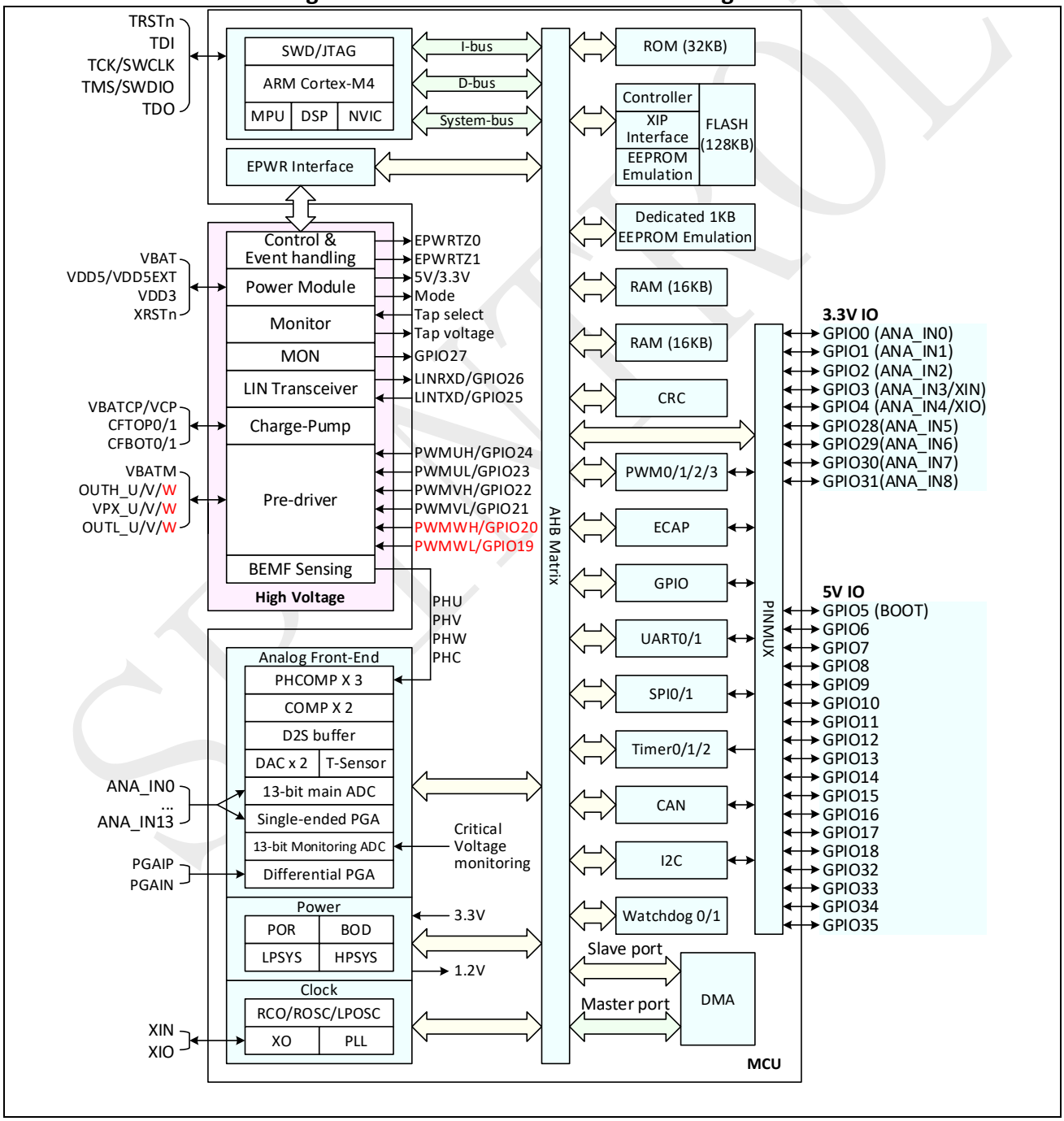
Terms or abbreviations

Terms or abbreviations	Description

1 SPD1179 Peripheral element selection

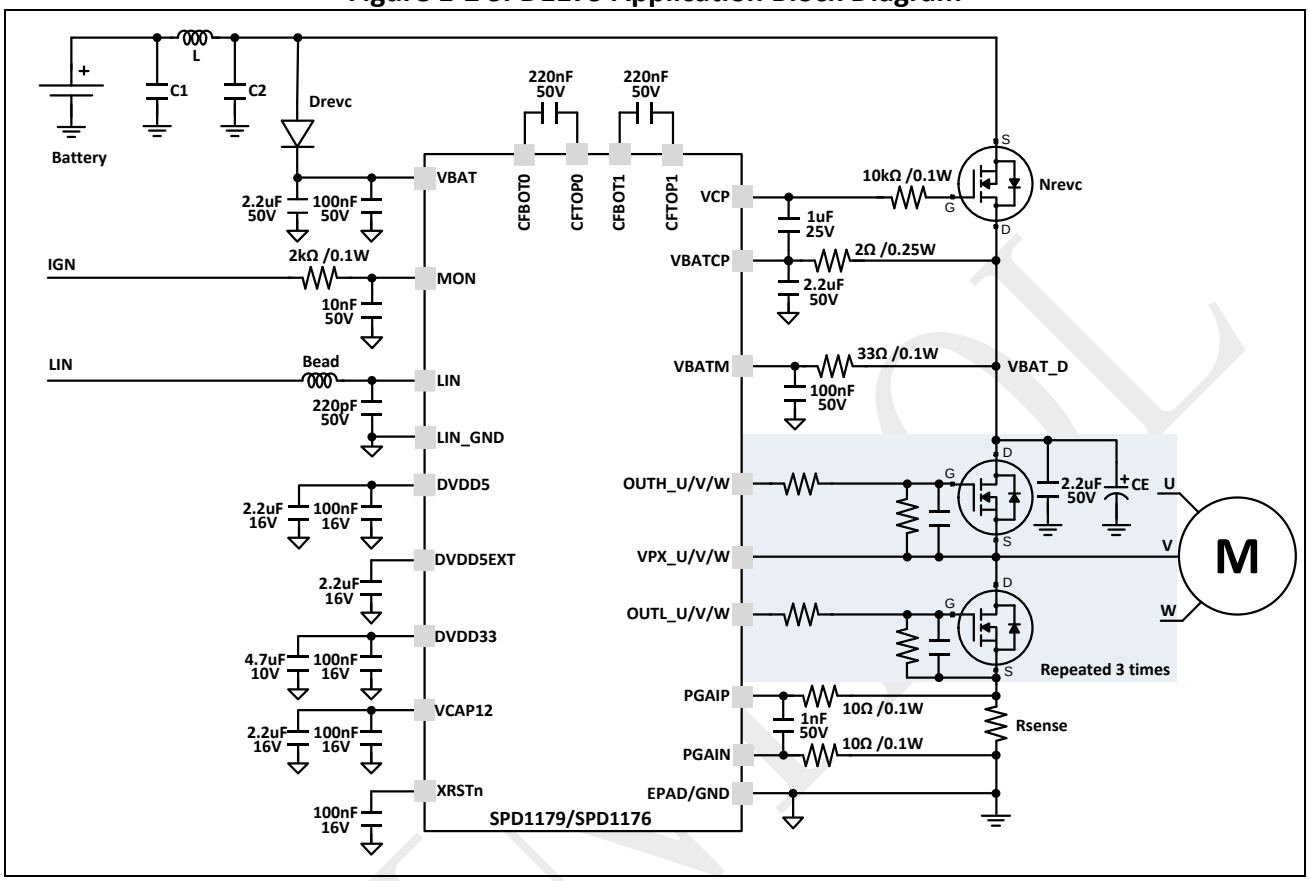
As shown in Figure 1-1, the SPD1179 chip mainly consists of MCU and High Voltage. The MCU part includes all the peripheral modules, which are classified according to functions, including ARM debugging interface module, 3.3V IO module, 5V IO module, crystal oscillator module, ADC sampling module and monitoring and protection module. The High Voltage part mainly includes power management module, MON wake-up module, LIN transceiver module, two-level charge pump module and three-phase bridge driver module. This section mainly explains the peripheral component selection method of the chip's various functional modules.

Figure 1-1 SPD1179 Functional Block Diagram



As shown in Figure 1-2, the basic peripheral circuit diagram of SPD1179 and the recommended device selection value. If there is no special need, please build the peripheral circuit of SPD1179 according to the recommended parameters in the diagram.

Figure 1-2 SPD1179 Application Block Diagram



Next, the selection criteria of device parameters for each module in the SPD1179 application block diagram are explained in detail, mainly including the following parts:

- Debugging and Downloading Interface Circuit
- External Crystal Oscillator Input Circuit
- Some Power Management Peripheral Circuit
- Pre-driving Chip Charge Pump Peripheral Circuit
- Pre-driving Chip Three-phase Bridge Driving Peripheral Circuit
- Single Resistor Sampling Input Circuit
- LIN Interface Circuit
- MON Interface Circuit
- Precautions for Use of IO Port

1.1 Debug and download interface circuits

SPD1179 debugging interface is ARM SWJ-DP Interface, which is a standard ARM CoreSight debugging interface, including JTAG-DP Interface (5 pins) and SW-DP Interface (2 pins). SPD1179 can also close the debugging interface through software. The pin definition of debugging function interface is shown in Table 1-1.

Table 1-1 SPD1179 MCU Debug Interface Pin Definition On Chip

SWJ-DP Port Pin Name	JTAG Debugging Interface		SW Debugging Interface		Instructions
	Type	Debugging Function	Type	Debugging Function	
GPIO15/ TDI/5V	Input	JTAG Data Input	-	-	When TRSTn is high, the debugging function is turned on, and the pins are defined in Table 1-2 below.
GPIO16/ TDO/5V	Output	JTAG Data Output	-	-	When TRSTn is high, the debugging function is turned on, and the pins are defined in Table 1-2 below.
GPIO17/ TMS/SWD/5V	Input	JTAG Mode Selection	Input / Output	Serial Data Input/Output	When TRSTn is high, the debugging function is turned on, and the pins are defined in Table 1-2 below.
GPIO18/ TCK/SWCK/5V	Input	JTAG Clock	Input	Serial Clock	When TRSTn is high, the debugging function is turned on, and the pins are defined in Table 1-2 below.
TRSTn/5V	Input	JTAG Module Reset	-	-	JTAG reset pin.

1.1.1 TRSTn

The TRSTn pin does not have the default pull-up or pull-down function inside the chip, and must be configured as pull-up to VDD5 or pull-down to GND by external circuit. When TRSTn is externally pulled up to VDD5, the chip debugging function is enabled, and the functions of the debugging port GPIO15~18 are shown in Table 1-2. When TRSTn is externally pulled down to GND by external circuit, the chip debugging function is disabled, GPIO15~18 as a common IO port, the chip can not be burned and can not be debugged.

Table 1-2 Debugging Interface Definition

Pin	Serial Line Debug Mode （Open SWV[1]）	Serial Line Debug Mode （Close SWV[2]）	JTAG Mode[3]

GPIO15	Function of user software configuration	Function of user software configuration	TDI
GPIO16	SWV	Function of user software configuration	TDO
GPIO17	SWD	SWD	TMS
GPIO18	SWCK	SWCK	TCK

[1] In the default state after the chip is powered on , GPIO15 is a general IO port and GPIO16 is a SWV function by default.

[2] Add this code: CoreDebug->DEMCR &= ~(1UL<<24), GPIO15 and GPIO16 can be used as general IO ports.

[3] Add this code: SYSTEM->DBGIFCTL = 1, enable JTAG mode.

1.1.2 GPIO5/BOOT

The pin level state of SPD1179 can select two jump start modes after Power On Reset (POR) through GPIO5/BOOT/5V (the chip is pulled down to GND by default inside the chip):

- When the BOOT pin is low at power-on reset, the SPD1179 program starts running from the internal Flash;
- When the BOOT pin is high at power-on reset, the SPD1179 program enters ISP mode, and GPIO10 is configured as UART_TXD function; GPIO11 is configured as UART_RXD function.

GPIO5/BOOT/5V pin can also be configured as a general IO port function, at this time, special attention should be paid to the pin level state of this pin must be low at the moment of power reset (POR release) to ensure that the chip can enter the Flash to start running the program, and only recommend as output IO function.

It is generally recommended that customers pull GPIO5/BOOT/5V pin down to ground through a 10K ohm resistor on the board. At this time, the chip will jump to the Flash to start executing the program after power reset. Pull TRSTn/5V up to DVDD5 through a 10K ohm resistor, at this time, the chip debugging function is enabled, GPIO15, GPIO16 can be used as general IO port, GPIO17, GPIO18 are respectively used as SWD, SWCK debugging pins.

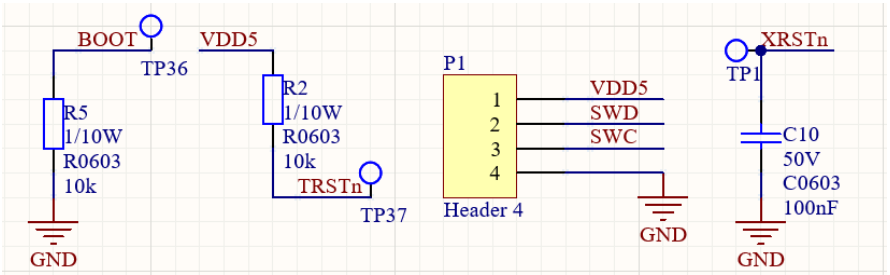
1.1.3 XRSTn

The XRSTn pin of SPD1179 is the global reset pin of the chip, and when it is at low level, all the functional modules of the chip will be reset. The XRSTn pin has a debounce circuit inside the chip, which can set the low level debounce time to 500us~4ms, and the chip will only be effectively reset when the low level of XRSTn exceeds this time. In addition, when the effective low level of XRSTn lasts more than 5s, it will further trigger the reset of all power modules, which is equivalent to power-on reset.

In addition to the pin reset, SPD1179 also has a power-on reset (POR) mechanism to ensure the power-on sequence of the chip, so it is generally not necessary to use the reset function of XRSTn. It is generally recommended that the XRSTn pin place a 100nF decoupling capacitor to GND, and place it close to the chip.

Figure 1-3 below shows the recommended circuit diagram of the SPD1179 debug and download interface. If there is no special requirement, please follow this recommended circuit diagram for design.

Figure 1-3 SPD1179 Recommended Debug And Download Interface Circuits



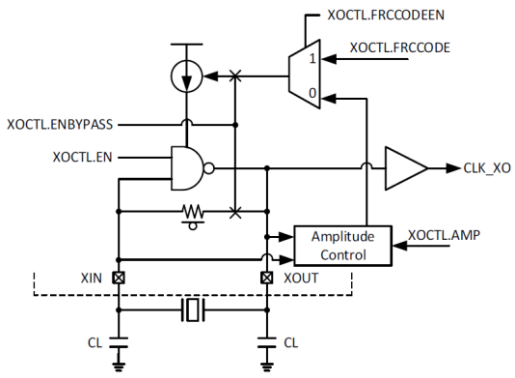
Note:	There are two methods of mass production burning for chip on board: 1. The recommended burning method is to power the chip VBAT directly (above 5V) and then burn it through the SWD, SWCK interface. 2. Provide 5.5V voltage at the VDD5 pin of the chip (it is recommended to use the burner provided by Xunzhi or the third-party burner recommended by Xunzhi), and then burn it through the SWD, SWCK interface.

1.2 External crystal oscillator input circuit

The SPD1179 chip has two internal RC oscillators, RCO0 is a factory-calibrated 32MHz internal RC clock (clock frequency error ±1.5% across the full temperature range) that can be used as an input to the PLL; RCO1 is a 32M internal RC clock, which is a backup clock for safety. XO is the clock input from external crystal oscillator or external clock source. PLL can provide up to 100MHz internal clock. For most occasions with low clock frequency requirements, the RCO0 clock inside the chip can be used directly.

For applications with high real-time requirements such as CAN communication, an external passive crystal oscillator is required. The external crystal oscillator input circuit diagram is shown in Figure 1-4， The chip integrates a 1M ohm feedback resistor, and only needs to be externally added with a passive crystal oscillator and two load capacitors. The frequency of the external passive crystal oscillator is 4-56MHz, and the load capacitor is 12pF-27pF. The selection of the crystal oscillator capacitor should refer to the recommendation of the crystal oscillator supplier, or it can be determined by the crystal oscillator startup test.Different external crystal oscillator needs software to set different input divider ratio, please refer to Section 3.7 of RC-034-2308001_SPD1179 Technical Reference Manual. When using external crystal oscillator, please must call our SDK function, or refer to Demo example.

Figure 1-4 External Passive Crystal Input Circuit



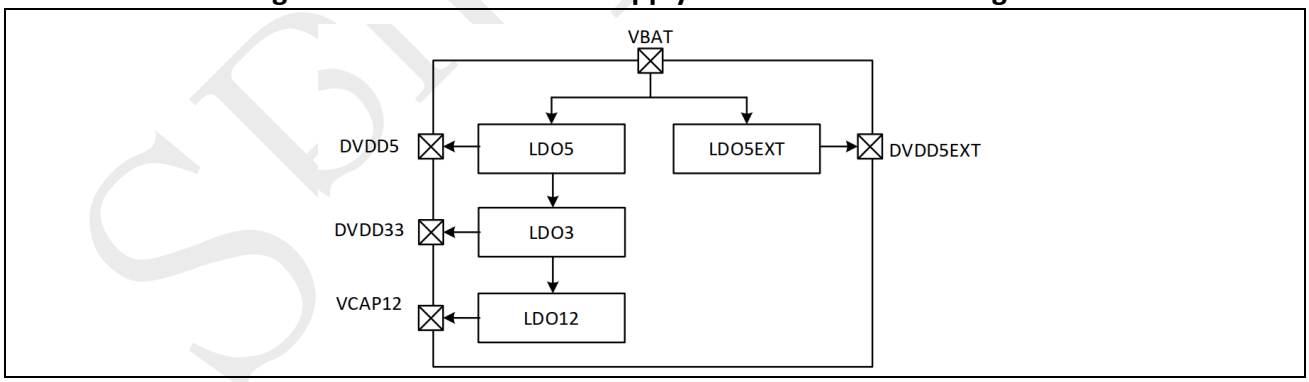
1.3 VBAT (MCU) part of the power management peripheral circuit

Figure 1-5 shows the MCU control part of SPD1179 power supply architecture block diagram. The MCU and control part of SPD1179 only need to be powered by a single power supply of 5.5V-40V from VBAT, and then use the internal cascaded LDO to generate the DVDD5 power supply (5V, 80mA) from VBAT, the DVDD33 power supply (3.3V, 50mA) from DVDD5, and the core power supply VCAP12 (1.2V, 40mA) from DVDD33. At the same time, the chip also integrates an independent LDO to generate the DVDD5EXT (5V, 40mA) from VBAT to supply external sensors.

Note:
1. External CAN transceiver chip needs to use external LDO for power supply.
2. DVDD5 and DVDD33 of the chip are power supplies for the internal circuit of the chip, and it is not recommended to supply external loads. If it is necessary to use them, please evaluate the size of the external load current requirement, control the external output current within 2mA, and consider whether the external load will short circuit or overvoltage and other extreme conditions, so as not to affect the normal operation of the MCU. In addition, the chip's driving ability of 5V, 3.3V and 1.2V is very weak in Stop mode, only 2-3mA, which can only drive the internal circuit, and at this time it is impossible to power the external circuit.
3. VDD5EXT is recommended for external power supply.

The power management module (PMU) inside the SPD1179 chip controls the generation and supply of all power, and there are three power modes controlled by the software state machine, namely Active Mode, Stop Mode and Sleep Mode. Please note that in Stop mode, the 5V, 3.3V and 1.2V LDO enter low power mode, and do not have the ability to output current externally. In Sleep mode, the output of 5V, 3.3V and 1.2V is shut off to 0V. For the functions and switching of these three power modes, and the wake-up logic of the chip from Sleep or Stop state, please refer to Section 2.2 of *RC-034_SPD1179 Technical Reference Manual*.

Figure 1-5 SPD1179 PowerSupply Architecture Block Diagram

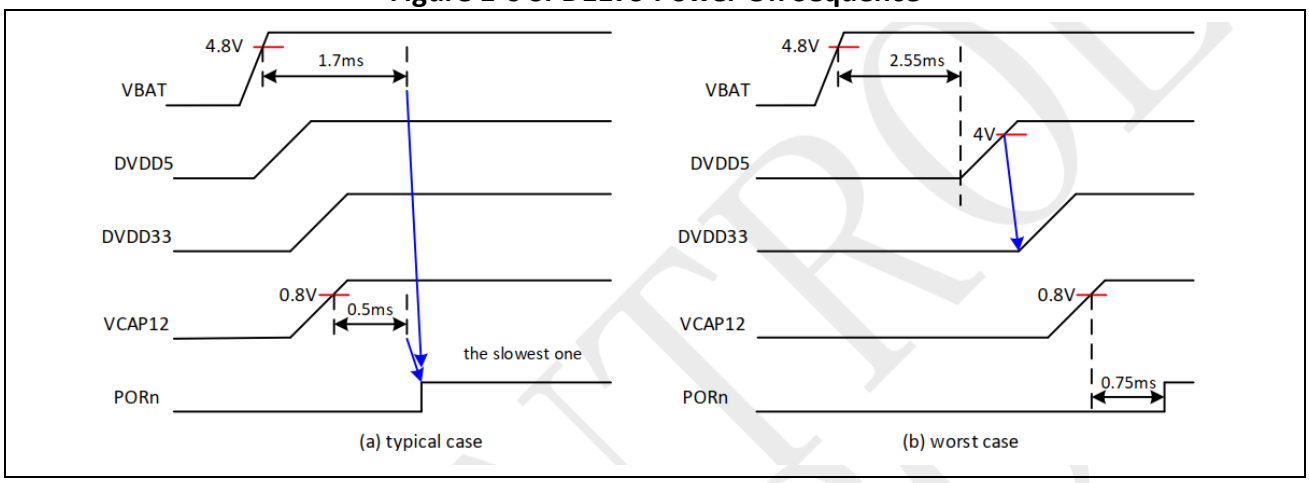


As shown in Figure 1-6, the SPD1179 has an integrated power-on reset module, which can ensure that the power-on sequence of each power supply of the chip meets the requirements. Figure 1-6(a) shows a typical power-on sequence. Typical case refers to junction temperature of 50 degrees Celsius, LDO load capacitance of 2.2uF, and chip batch of typical batch. When VBAT is powered on, DVDD5 and DVDD3 follow VBAT to power on. VCAP12 follows VDD33 to power on. The condition for PORn release of MCU core logic is that VBAT rises to 4.8V for 1.7ms and VCAP12 rises to 0.8V for 0.5ms. After PORn is released, SPD1179 enters active mode.

The worst-case power-on sequence is shown in Figure 1-6(b). The worst case refers to junction temperature of 150 degrees Celsius, LDO load capacitance of 4.7uF, and chip batch of slowest batch.

After VBAT rises to 4.8V, after a stable time of 2.55ms, DVDD5 starts to power on. When DVDD5 rises to 4V, DVDD5 is ready to trigger DVDD33 and VCAP12 to power on. When VCAP12 rises to 0.8V, after 0.75ms, MCU core logic PORn is released. SPD1179 enters active mode.

Figure 1-6 SPD1179 Power On Sequence



Due to the single power supply design of the SPD1179, the design of the peripheral circuit of the power supply is greatly simplified, only needing to add decoupling capacitors near the corresponding power supply pins and GND (EPAD), that is, adding decoupling capacitors near the chip pins of VBAT, DVDD5, DVDD33, VCAP12, DVDD5EXT and GND (EPAD). The capacitance selection is analyzed below.

1.3.1 VBAT peripheral circuit

VBAT is the power input pin of SPD1179, and the MCU and internal logic control power supply are generated through the internal cascaded LDO. It is recommended to add a 2.2uF/50V+100nF/50V decoupling ceramic capacitor at the power input pin to reduce the input power ripple.

Note: In some applications that require power down storage of the EEROM, the VBAT pin will place a large-capacity electrolytic capacitor, the capacity of which is determined based on the following information:
①SPD1179 pre-drive stop only the MCU running current consumption is about 40mA, corresponding to the waiting time between writing EEROM
②the software frequency reduction is performed, the main frequency of 100M is reduced to 24M; at the same time, the ADC module is closed, and only the relevant modules of writing EEROM are retained. At this time, the chip current consumption is about 20mA
③SPD1179 takes 42us to write one Word in EEROM.
For details about how to write EEROM, please refer to *the SPD1179 EEROM Usage Guide*.

As shown in Figure 1-2 above, The chip VBAT power supply is usually powered by an independent anti-reverse diode, not shared with the main power anti-reverse MOSFET, because when the external input power is suddenly cut off, due to the power consumption of the motor rotation, the DC bus voltage will drop quickly, and VBAT will not drop quickly because it uses a separate anti-reverse diode.

It is recommended that the VBAT power supply position of the chip be placed behind the CLC filter circuit input at the power port, in front of the main power anti-reverse MOSFET, and the PCB lead line position be in the positive terminal of the filter capacitor, far away from the position with large switching noise. The DEMO board uses this connection mode.

1.3.2 DVDD5、DVDD33、VCAP12 Capacitors

2.2uF+100nF decoupling ceramic capacitor to DVDD5, with a minimum withstand voltage of 10V, and the value range of the DVDD5 port capacitor is 2.2uF~4.7uF.

It is recommended to add a 4.7uF+100nF decoupling ceramic capacitor to DVDD33, with a minimum withstand voltage of 10V.

It is recommended to add a 2.2uF+100nF decoupling ceramic capacitor to VCAP12, with a minimum withstand voltage of 10V, and the value range of the VCAP12 port capacitor is 1uF~4.7uF.

Note: The DVDD33 port capacitor is recommended to be placed at 4.7uF, which can ensure the stable establishment of the power system.

1.3.3 DVDD5EXT Capacitor

It is recommended to add a 2.2uF+100nF decoupling ceramic capacitor to DVDD5EXT, and the minimum withstand voltage is recommended to be 10V. The capacitance value range of DVDD5EXT port is 1uF~4.7uF.

Note：
1. DDVDD5EXT port capacitance ranges from 1uF to 4.7uF. Please do not place more than 4.7uF capacitance in this pin, which may cause the power supply to fail to be established.
2. If you do not use VDD5EXT, you need to turn off the VDD5EXT LDO and add 100R-1K load resistor to the VDD5EXT output to avoid overvoltage of the VDD5EXT output, resulting in internal ESD damage to the VDD5EXT.

The selection summary of the capacitance of the SPD1179 chip peripheral decoupling capacitor is shown in Table 1-3 below.

Table 1-3 Recommended Value Of The Decoupling Capacitor In The Power Domain Of SPD1179 Chip

Signal name	Type	Description
VBAT	Power Source	The chip has a single power input, and a high frequency decoupling capacitor of 2.2uF+100nF (50V) is placed near the VBAT and GND pins.
DVDD5	Power Source	Digital power supply, 2.2uF+100nF (10V/16V) high frequency decoupling capacitor is placed near DVDD5 and GND.
DVDD33	Power Source	The MCU analog power supply is 3.3V, and a high-frequency decoupling capacitor of 4.7uF+100nF (10V) is placed near the DVDD33 and GND.
VCAP12	Power Source	The core is 1.2V, and a high-frequency decoupling capacitor of 2.2uF+100nF (10V) is placed near the VCAP12 and GND.
DVDD5EXT	Power Source	The 5V external sensor is powered, and a 2.2uF+100nF (10V/16V) high frequency decoupling capacitor is placed near the DVDD5EXT and GND.
EPAD	Chip Reference Site	The GND plane of the chip and the two GND pins of the chip also need to be directly connected to the

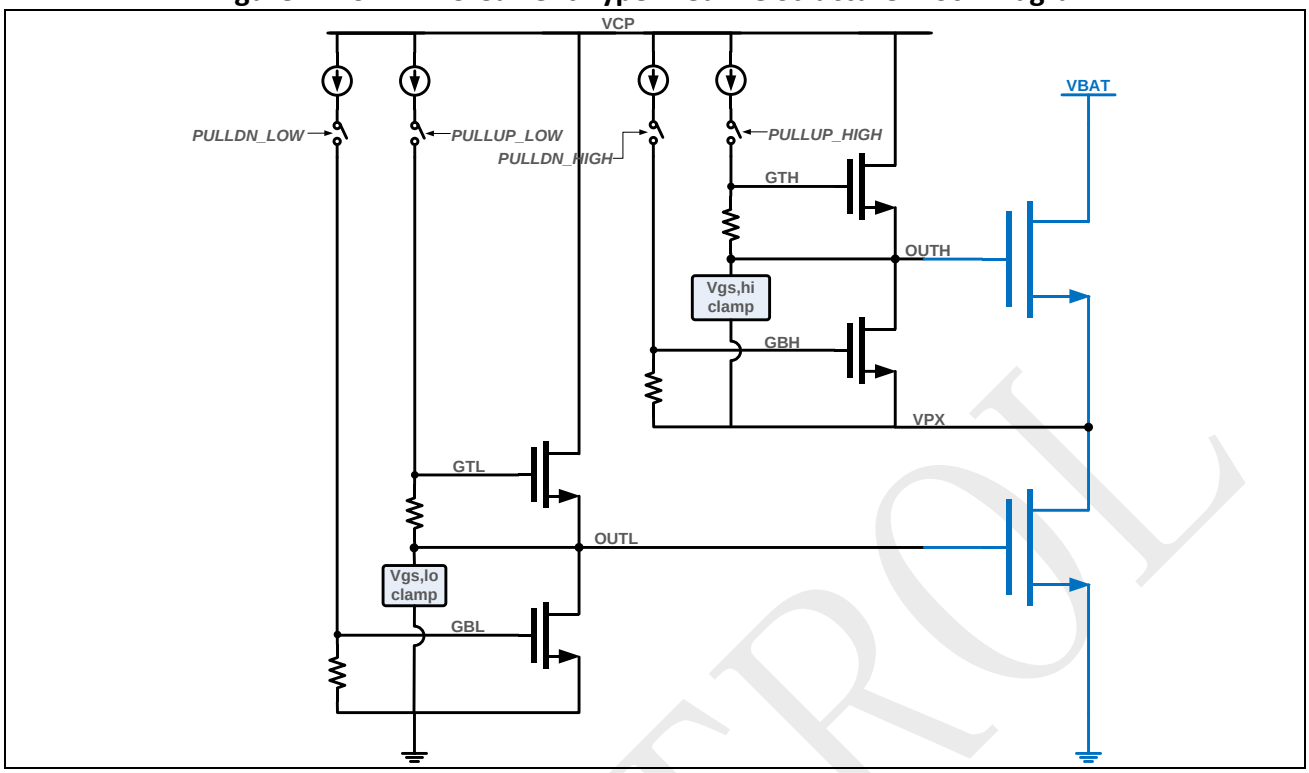
		EPAD. All power decoupling filter capacitors of the chip must be connected to the EPAD with low impedance. The EPAD is a chip heat dissipation pad and needs to be connected to the ground plane through multiple holes. Pay attention to the reliability of welding.
VBATM	Power Source	Place a 100nF high-frequency decoupling capacitor close to the VBATM and GND pins between the three-phase bridge power input measurement pins.
VBATCP	Power Source	Charge pump power input pin, a 2.2uF (50V) high frequency decoupling capacitor is placed near VBATCP and GND.
VCP	Power Source	Charge pump power output, a 2.2uF (25V) high frequency decoupling capacitor is placed near the VCP and VBATCP.

1.4 Pre-drive chip charge pump part of the peripheral circuit

Numbers with an asterisk (*) indicate that the value is a chip design value and is not used as a card test standard during production.

The SPD1179 three-phase bridge driver is a current-type driver, as shown below Figure 1-7, which is significantly different from voltage-type drivers (with self-lifting capacitors). Hardware saves three self-lifting diodes and self-lifting capacitors. The current-type pre-driver uses two-stage charge pumps to generate a high-voltage VCP power supply based on the bus voltage. Then use the VCP power supply to generate 12 adjustable constant current sources to drive the chip's internal MOSFET drive output stage, and then drive 6 external three-phase bridge MOSFETs, so after the charge pump output voltage VCP is ready, you can open any MOSFET, no boot-up charging and other logical restrictions, the High-side bridge can be turned on 100%.

Figure 1-7 SPD1179 Current Type Predrive Structure Block Diagram



1.4.1 Charge pump flying capacitor CF0, CF1 and charge pump regulator capacitor Cvcp

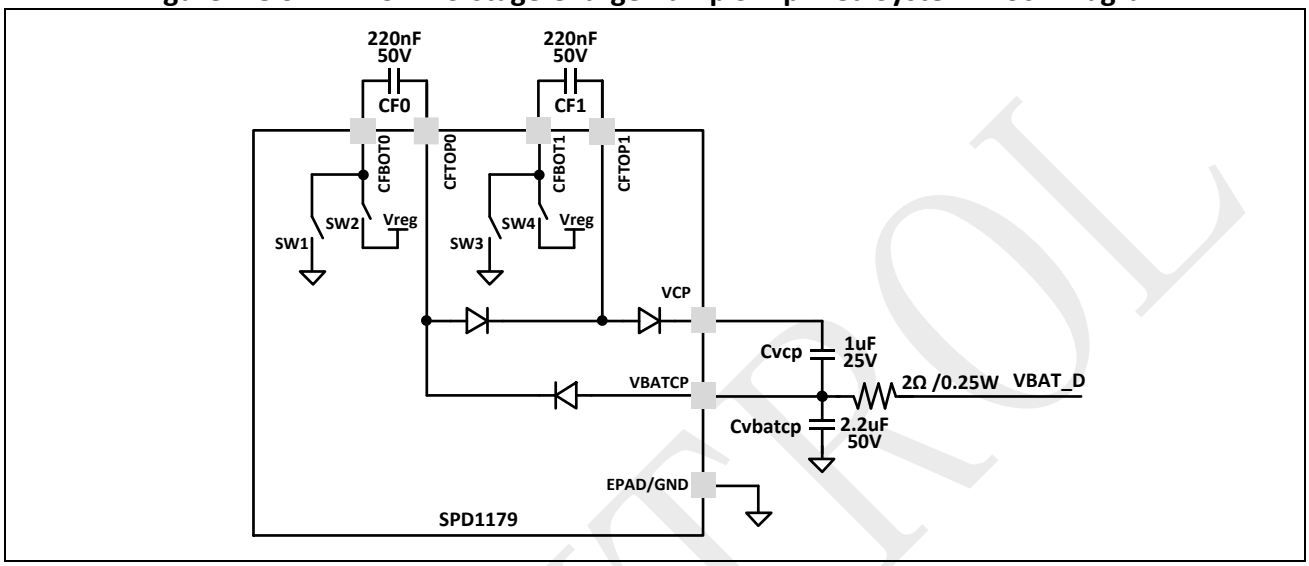
As analyzed above, the core of SPD1179 current-type pre-drive is a two-stage charge pump circuit, which uses two-stage charge pumps to generate VCP voltage (default value, software adjustable VCP voltage) higher than the three-phase bridge bus voltage 12V, and then uses VCP voltage to generate 6 controllable current sources for driving and controlling the GS voltage of the three-phase bridge. The two-stage charge pump can provide higher output voltage, and can provide enough VCP voltage when the charge pump power input voltage VBATCP is as low as 5.5V (when the car is cold start), so as to ensure the normal operation of the three-phase bridge under low voltage.

Figure 1-8 shows the system block diagram of SPD1179 two-stage charge pump. The peripheral circuit design of charge pump requires the selection of appropriate two-stage charge pump flying capacitors CF0, CF1 and charge pump voltage regulator capacitors Cvcp. The principle of charge pump is to use the high frequency action of the internal charge pump switch (equivalent switching frequency 312kHz*) to continuously switch the flying capacitor in the following two loops: ① from the VBATCP charging loop; ② Fully charged flying capacitor + register configurable reference voltage Vreg backstage circuit discharge loop. The voltage on the charge pump flying capacitor does not change during loop switching, and the VCP voltage is generated by using the accumulated voltage (charge) on the flying capacitor + two Vreg voltage increases. So, VCP voltage =VBATCP +2*Vreg-3*VDiode. The software default set charge pump output voltage is higher than the VBATCP voltage 12V, that is, 2*Vreg=12V, typically 3*VDiode=2.1V, then when the VBATCP voltage is equal to 12V, the VCP voltage is equal to about 21.9V.

Note:	The charge pump of SPD1179 has frequency spreading function. When EMC regulation is carried out, it is necessary to confirm whether the frequency spreading function of

charge pump is turned on. The confirmation method is to measure the waveform of CFBOT to GND. Without frequency spreading, it is about 312k*, and with frequency spreading, it is from 156k* to 312k* fluctuating frequency. The latest software support package (SDK) program, the frequency spreading function of charge pump is turned on by default. This is beneficial for passing EMC tests.

Figure 1-8 SPD1179 Two-stage Charge Pump Simplified System Block Diagram



The selection of CF0 and CF1 will consider the following aspects: ① If the selection is too small, the amount of charge stored on the flying capacitor will be reduced, and the total charge output to VCP under the same switching frequency will be reduced. When VCP needs to output a larger driving current, the VCP voltage will drop, that is, the load capacity of the charge pump is not enough, and it cannot output relatively large driving current.②If the flying capacitor is selected too large, it will take longer to fill VCP under the same charge pump switching frequency, that is, the dynamic response ability of VCP will be worse. But the large CF capacitor can output larger current, under the same driving output current, the drop of VCP voltage will be lower. At the same time, the CF capacitor is also a 50V withstand voltage capacitor as the bus, and the large capacity capacitor is also more expensive.

Cvcp capacitor is used to stabilize the output VCP voltage of the charge pump, ensure the stability of the three-phase bridge driving current output, and when the VBATCP voltage suddenly fluctuates, due to the presence of this voltage-stabilizing capacitor, the VCP voltage will follow the VBATCP voltage fluctuation, which can also ensure the driving voltage stability of the high-side bridge MOSFET. The Cvcp capacitor can also be adjusted appropriately according to the actual test of VCP ripple.

Based on the above analysis and the actual charge pump load capacity tests, Spintrol recommend 220nF/50V for CF0 and CF1 and 2.2uF/25V for Cvcp for most applications.

Note: Cvcp capacitors need to be placed between VCP-VBATCP to stabilize the voltage between VCP-VBATCP.

1.4.2 VBATCP peripheral circuit

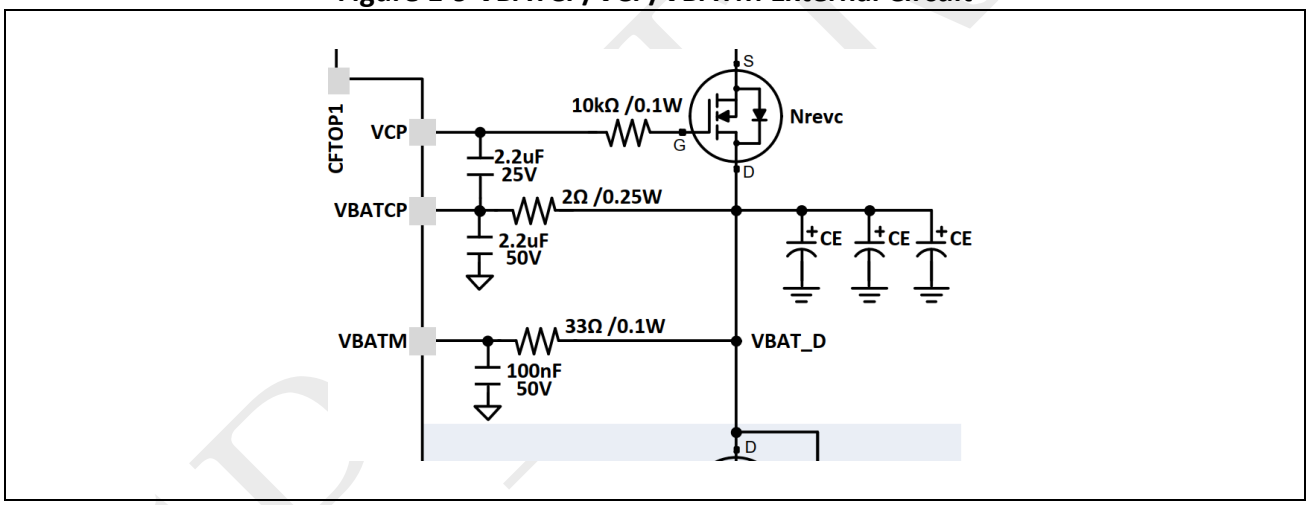
VBATCP is the input power supply of charge pump, so the value must be much larger than the charge pump flying capacitor. In general, the larger the capacitance, the smaller the input voltage ripple. Considering the convenience of component selection, it is recommended to place 2.2uF/50V capacitor at the VBATCP port, and to choose a low ESR ceramic capacitor, and the PCB is placed near the chip pin.

In general, in motor drive applications, VBATCP is connected to the bus power supply VBAT_D of the three-phase bridge. It is recommended to connect a 2R/0.25W resistor in series for filtering to prevent some high-frequency peak voltages on the three-phase bridge bus from damaging the internal ESD devices of the chip. At the same time, it is recommended that the VBATCP power supply lead from the positive terminal of the bus capacitor on the PCB, which can reduce the switching ripple.

Note:	Evaluate the power of the 2R resistor in series according to the actual ripple condition. It is recommended to use a 1206 package with 0.25W power resistance.

Figure 1-9 is the external circuit of the recommended VBATCP pin.

Figure 1-9 VBATCP/VCP/VBATM External Circuit



1.4.3 VBATM peripheral circuit

The VBATM pin is a measurement pin for the D-pole voltage of the high-side-bridge MOSFET, and it is recommended to series 33 ohm resistor and add a 100nF filter capacitor to the chip pin. The accurate measurement of the D-pole voltage of the high-side-bridge MOSFET is for the Vds overvoltage detection function of the high-side-bridge MOSFET. This measuring pin has almost no input current, it is recommended that PCB wiring from the V phase MOS D pole to walk a separate thin measuring wire, do not share with the VBATCP power supply wire.

1.4.4 Charge pump carrying capacity and Qg size of external MOSFET capable of driving

Test the charge pump output load capability as described in Section 27.2 of the *RC-034_SPD1179 Technical Reference Manual*, where VCP outputs a constant 12mA current with a charge pump flying capacitor of 100nF, and the VCP-VBATCP voltage still meets the requirements of the three-phase bridge drive when VBATCP voltage drops to 5.5V.

In the case of a constant 12mA output current, you can simply estimate the Qg size of the external three-phase bridge MOSFETs that can be driven. If the switching frequency of the commonly used three-phase bridge is selected as 16kHz, the switching period T3HSW is 62.5us. The amount of charge Q1 that VCP can output in a switching cycle is:

$$Q_1 = I_{charge\ pump} * T_{SW} = 12mA * 62.5us = 750nC \quad \textbf{Formula 1.1}$$

Select the commonly used seven-stage SVPWM modulation mode, there will be a total of 6 MOSFET opening process in each switching cycle, assuming that the Qg required for MOSFEF opening is Qg_mos, then the total gate level opening drive charge demand is 6*Qg_mos. In the process of MOSFET maintenance, the current required to provide the MOSFET is very small, assuming that the total on-maintenance current is 800uA, then the maintenance on-charge required to provide in the switching cycle is 800uA*62.5us=50nC; Each switching cycle will have 6 MOSFET shutdown, MOSFET shutdown needs to provide very small energy, because driving the external MOSFET shutdown only need to drive the pre-drive output stage pull down MOSFET open, take the turn-off energy is 20nC, then the total charge Q2 consumed by the three-phase bridge drive in a switching cycle is:

$$Q_2 = 6 * Q_{g_{mos}} + 50nC + 20nC \quad \textbf{Formula 1.2}$$

Assuming that the output charge of the charge pump in a switching period is equal to the charge required by the three-phase bridge drive, that is, the VCP voltage can maintain a stable voltage, then Q1=Q2, then Qg_mos=113nC can be calculated according to **Formula 1.1** and **Formula 1.2**. That is, the maximum external MOSFET that the SPD1179 charge pump can drive has a Qg of 115nC, note that this includes the amount of charge pump required to drive the MOSFET itself plus the amount of charge required for the capacitive charge applied by the MOSFET GS.

Note:	Current-type pre-driving is to provide the charge required for three-phase bridge MOSFET driving by two-stage charge pump, so when selecting MOSFET with very large Qg or increasing too much external capacitance on MOSFET GS, attention should be paid to the load capacity limit of the charge pump. In actual products, test the voltage of VCP-VBATCP and the voltage of Vgs of the three-phase bridge MOSFET.

1.5 The predrive chip is connected to the three-phase bridge MOSFET circuit

The HO_U/V/W of SPD1179 pre-driver output is the G-pole control signal of the three-phase high-side bridge MOSFET, and VPX_U/V/W is the S-pole signal of the three-phase high-side bridge MOSFET, which form the bridge drive circuit. LO_U/V/W is the control signal of the three-phase low-side bridge MOSFET, and the drive signal of the low-side bridge is referenced to the GND of the chip, which means that the drive circuit of the low-side bridge needs to pass through the sampling resistor to return to the GND of the chip.

Figure 1-10 shows the recommended three-phase bridge partial circuit.

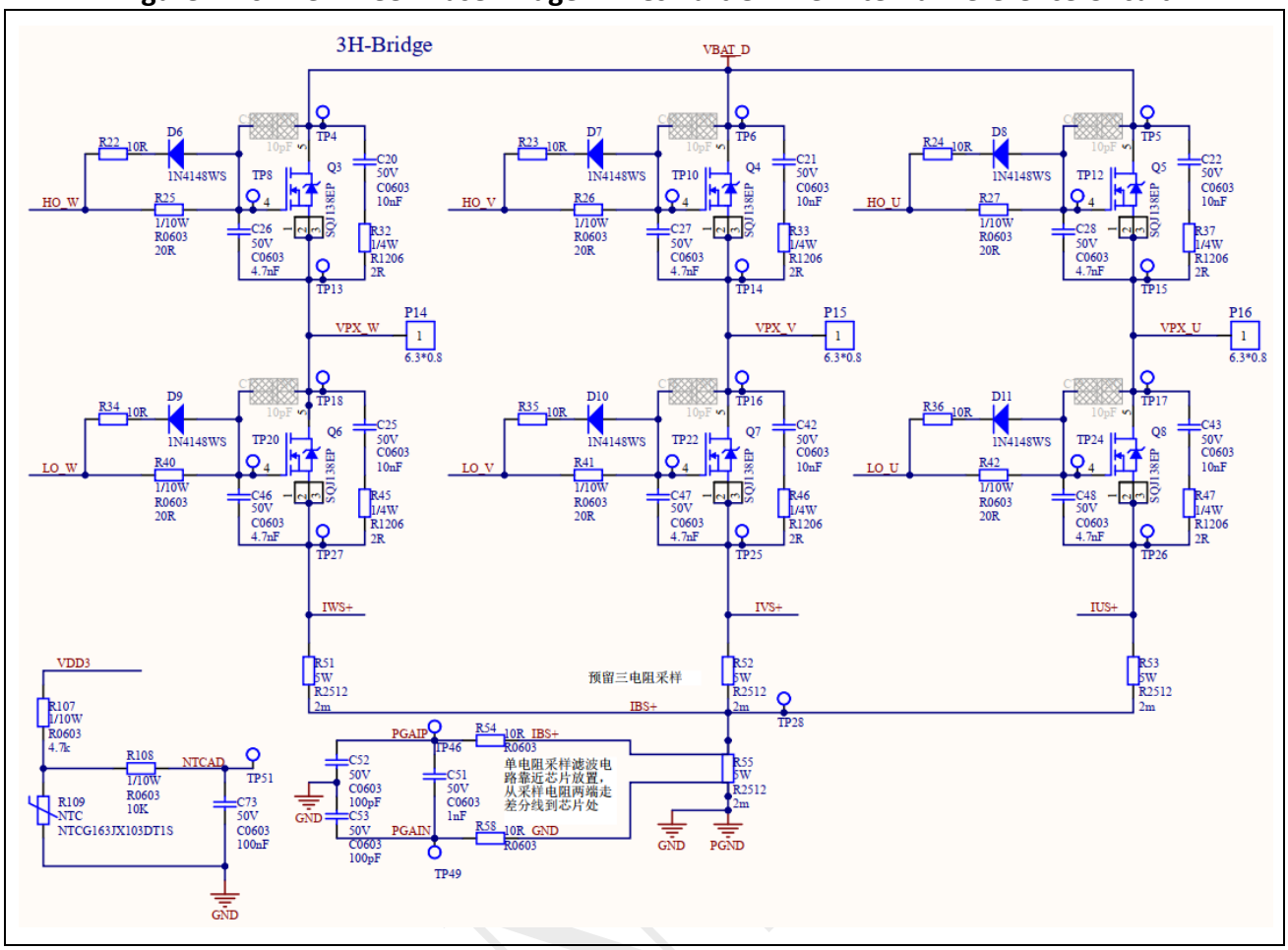
The three-phase bridge MOSFET driver resistance is recommended to be placed 10-51 ohms, and the value of this driver resistance is adjusted according to the requirements of the switching speed. MOSFET GS capacitor needs to be combined with the MOSFET's own Cgs capacitor selection, generally increase the Cgs capacitor is to improve the MOSFET Vgs drive waveform, while stabilizing the GS voltage, to prevent the MOSFET from opening by mistake, here also need to pay attention to the MOSFET opening voltage Vgs(th), you are advised to select a MOSFET with Vgs(th) greater than

2V. However, excessive CGS capacitance will lead to an increase in the current required for driving. Please note that the total MOSFET Qg that SPD1179 can drive as simply estimated in Section 1.4 should be limited to about 115nC. If the driven MOSFET Qg is too large, it will lead to a drop in the high side bridge drive voltage. At the same time, the larger drive current will also cause the chip temperature rise to increase, which requires enhancing the heat dissipation capacity or limiting the ambient temperature, which is an unfavorable factor. A 65k pull-down resistor has been integrated in the chip between GS, which can not be added at the MOSFET (between HO_U/V/W and VPX_U/V/W in the chip, and between LO_U/V/W and GND has been integrated with 65k pull-down resistor). It is recommended to add an appropriate RC absorption circuit between the DS of the three-phase bridge MOSFETs to improve EMC characteristics. For MOSFETs with fast switching speeds (Qgs and Qgd are small), capacitors between GD can also be reserved for EMC debugging.

Using current-mode pre-driver can conveniently adjust the driving current of MOSFET and adjust the switching speed of MOSFET, so as to find the optimal solution between EMC performance, heat generation and system efficiency. Please test and adjust according to the actual circuit, and refer to *The Application Guide Of SPD1179* for more design details.

Note:	1. It is suggested to use drive resistor to adjust the switching speed of three-phase bridge MOSFET. 2. In addition to the configuration of MOSFET switching stage drive capability, the current type pre-driver also needs to configure the static current of the pre-driver, that is, the drive current of the pre-driver to maintain the high or low state of the external MOSFET. The default static current of the latest software support package (SDK) is 100mA. Increasing the static current will increase the current consumption of the pre-driver and the power consumption of the chip.

Figure 1-10 The Three Phase Bridge Drives Part Of The External Reference Circuit



1.5.1 Resistor sampling input circuit

As shown in Figure 1-10, the recommended sampling method for three-phase bridge current is single resistor sampling. Two difference wires (Kelvin lines) are drawn from both ends of the sampling resistor and go to the vicinity of MCU. Then the differential wire is connected to the filtering network composed of R54, R58 and C51, C52 and C53 in the figure, and directly input to the PGAIP and PGAIN pins of MCU. Filter resistors R54, R58 recommended to choose 10 ohms, the value is too large will affect the amplification of PGA inside the chip, so do not recommend customers to change this resistor value. The value of differential mode filter capacitor C51 is more critical, and it is generally recommended to use 1nF filter capacitor, and the time constant τ of differential mode filter is 20ns, which can meet the filtering requirements of most applications. When the sampling resistor value is small, the sampling resistance value is also small, the signal to noise ratio of the sampled signal is very poor, you can appropriately increase the value of C51 filter capacitor, such as 10nF, 100nF, please adjust according to the actual motor debugging and current sampling waveform. C52 and C53 are common mode filter capacitors, and the capacity is recommended to be 100pF, which can also be adjusted according to the actual situation. Filter resistors and capacitors should be placed close to the chip pins during PCB layout.

1.6 LIN interface circuit

The SPD1179 chip integrates a LIN communication module internally, which complies with LIN spec 2.2A and SAEJ2602-2 communication protocols, and the communication rate can reach up to 20kbps. During the chip program downloading, the LIN communication rate can reach up to 115.2kbps. LIN

signal can be used as the wake-up source for the chip to exit from Stop and Sleep modes. Generally, when the LIN input is lower than 0.5*VBAT voltage, the chip will be woken up. The LIN transmitter is integrated with overcurrent and overtemperature protection functions, TXD timeout detection functions, and TXD slope control functions.

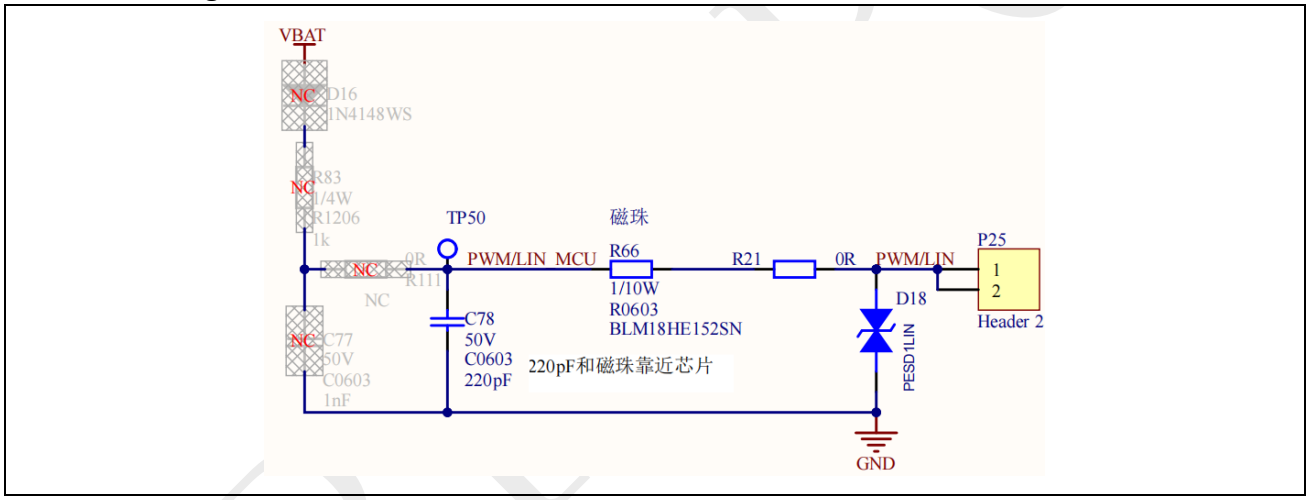
The parameter design requirements for the master and slave ends in the LIN network are shown in Table 1-4.

Table 1-4 Master and slave design parameters

Function	Pull-up resistance	Ground capacitance
Master	1K	1nF
Slave	30K	220pF

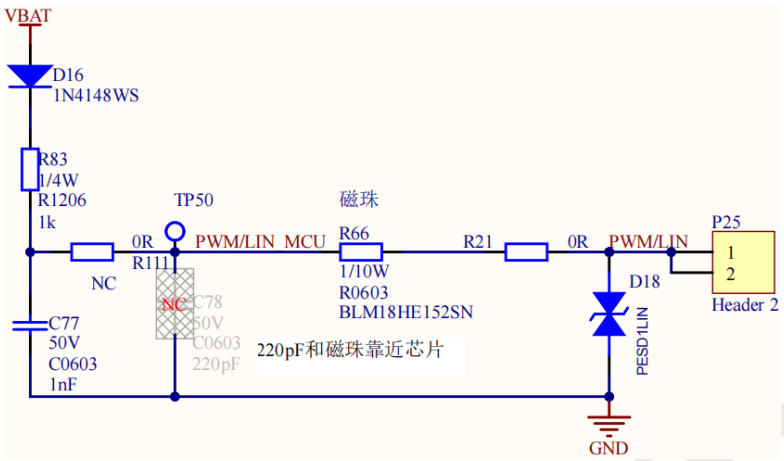
As shown in Figure 1-11, it is the recommended ciucuit for SPD1179 in slave mode of the LIN interface. In slave mode, only a 220pF capacitor is connected to the ground near the LIN pin, as shown in Figure 1-11 C78, and the R111 resistor is disconnected without welding. Because the chip has integrated a VBAT pull-up diode and a 30K ohm pull-up resistor between LIN pin and VBAT, there is no need to add an additional 30K ohm pull-up resistor.

Figure 1-11 SPD1179 LIN Interface Recommended Circuit in Slave Mode



As shown in Figure 1-12, it is the recommended circuit for SPD1179 in master mode of the LIN interface. In Master mode, it is necessary to select appropriate pull-up resistor and ground capacitor values to ensure that the waveform slope in LIN conformance test meets the specification requirements. Generally, 1K pull-up resistor and 1nF ground capacitor are used, as shown in R83 and C77 in Figure 1-12. In this case, the R111 resistor needs to be welded and the capacitor C78 needs to be removed.

Figure 1-12 SPD1179 LIN Interface Recommended Circuit in Master Mode



Note: Regardless of being a slave or a master, magnetic beads need to be added to the LIN port. The recommended model of magnetic beads is MMZ1608B102CT(or BLM18HE152SN1D). It is recommended to select a magnetic bead with larger impedance characteristics in a low frequency band, such as @1M. A 220 pF capacitor is needed between LIN port and the ground. The magnetic beads and capacitor should be put close to the chip pin. The ESD protection diode should be put close to the LIN signal connector port.

When the master and slave communicate with each other in LIN, the length of the connecting wire has certain influence on the LIN waveform. When the connection wires are long, the equivalent capacitance between the wires is greater than 1nF. In this case, the master does not need to attach an additional 1nF ground capacitor. You need to select an appropriate pull-up resistor based on the measured capacitance between the off-board wires. The relationship between the pull-up resistor at the master end and the value of the capacitor between the wires is shown in Table 1-5.

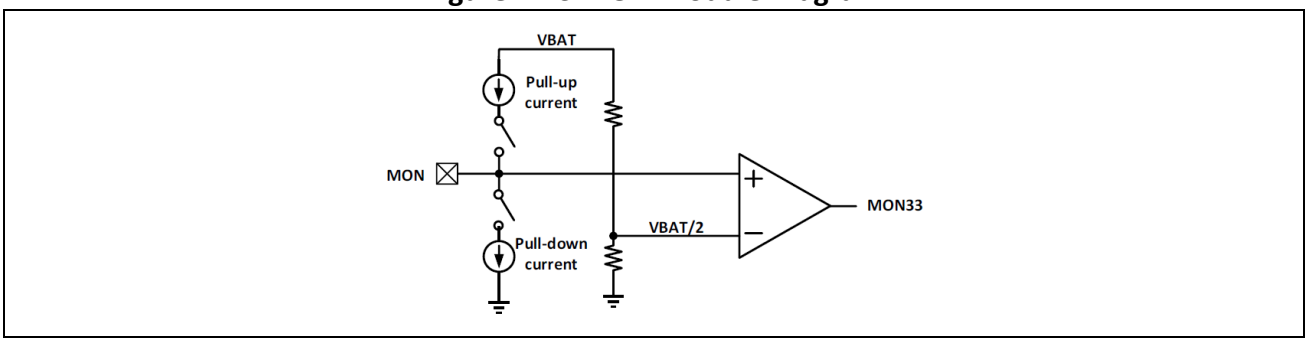
Table 1-5 Relationship between the pull-up resistor and the capacitance between the wires

Correspondence	Pull-up resistance	Interconductor capacitance
1	1K Ω	1nF
2	660 Ω	8nF
3	500 Ω	10nF

1.7 MON Interface circuit

As shown in Figure 1-13, The SPD1179 internal integrates a high voltage monitoring module (MON), which can monitor the voltage of the power supply or the external high voltage source higher or lower than the specified VBAT/2 threshold voltage, and the comparison result is directly fed into the MCU low voltage module for digital processing. The MON interface is internally integrated with pull-up and pull-down current sources. The pull-up current source can be configured by software to prevent the interference signal on the MON pin from causing the comparator to flip incorrectly by clamping the pull-up current source. The MON signal can be used as the signal source to wake up the chip from Stop and Sleep modes, and the high-level or low-level wake-up function is configurable. The MON interface can be directly connected to the KL15 high voltage wake-up source, and a 2k+10nF RC filter circuit can be added near the chip.

Figure 1-13 MON Module Diagram



1.8 Precautions for using the I/O port of SPD1179

1.8.1 I/O Port Drop-down by Default

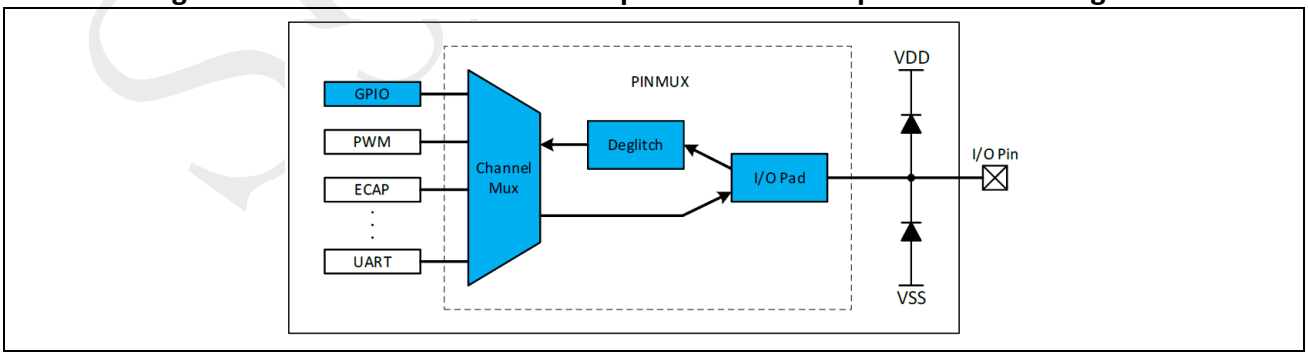
Please refer to Section 3.3 of *the RC-031_SPD1179_Datasheet* GPIO Pin Reset Function and Status. When designing the IO port circuit, please consider the internal pull-up and pull-down effects (pull-up and pull-down resistors 50k ohms) after power-on reset. Before software configuring the IO port pull-up and pull-down status, the internal default pull-up and pull-down status may cause the circuit to misoperate. Please avoid this situation. If necessary, external pull-up or pull-down resistors should be added to the IO port to make the chip in a certain level state before software configuring the IO status after power-on reset.

Note:	After power-on reset (POR), each IO port of SPD1179 has a default level state. When using the IO port to drive relays or switch loads, please note that this default state may cause the circuit to misoperate.

1.8.2 Integrated up-and-down clamp diode in I/O port

As shown in Figure 1-14, The up-and-down clamp diode is integrated inside the SPD1179 IO port. The voltage of the clamp diode inside the 5V IO port is 5V, and the voltage of the diode clamp inside the 3.3V IO port (analog port) is 3.3V.

Figure 1-14 SPD1179 Internal Pull Up And Down Clamp Diode Block Diagram



When the IO port input voltage is higher than the internal clamp supply voltage, then the diode clamp action will occur, there will be a feed current from the IO port into the 5V or 3.3V supply. This is often encountered in automotive key signal detection, where the high-level key signal is the battery voltage (9-16V) and the low-level is 0V.

Note:	When a high voltage must be directly input to the IO port, please note that a current-limiting resistor must be added to limit the current flowing into the chip's internal power supply. Please keep the total current flowing into the chip's internal power supply below 5mA.

The reason for limiting the current flowing from the IO port to the chip's internal 5V or 3.3V power supply is that the 5V or 3.3V power supply inside the chip is the output of the internal LDO, which does not have the ability to pull down and discharge. If the current flowing into 5V or 3.3V is greater than the power consumption of the power domain itself, then 5V or 3.3V will be overcharged, which will cause the chip's power supply to be overvoltage and damaged or the chip's function to be abnormal, which is not allowed.

1.8.3 The high voltage on the I/O port in the sleep mode of the chip will generate static power consumption

Note:	In sleep mode, the chip needs to cut off the high voltage input to the IO port through the switching circuit, and it is not allowed to continue to inject current into the IO port in sleep mode. Because the current injected into the IO port in sleep mode will increase the static power consumption of the system.

This chapter explains the recommended circuit and component selection method according to the peripheral circuit of SPD1179 chip one by one by module. Please check whether the peripheral circuit configuration is reasonable according to these modules when designing the schematic diagram or reviewing the schematic diagram.

2 SPD1179 Recommended circuits for other applications

2.1 SPD1179 power input filter and high border reverse circuit

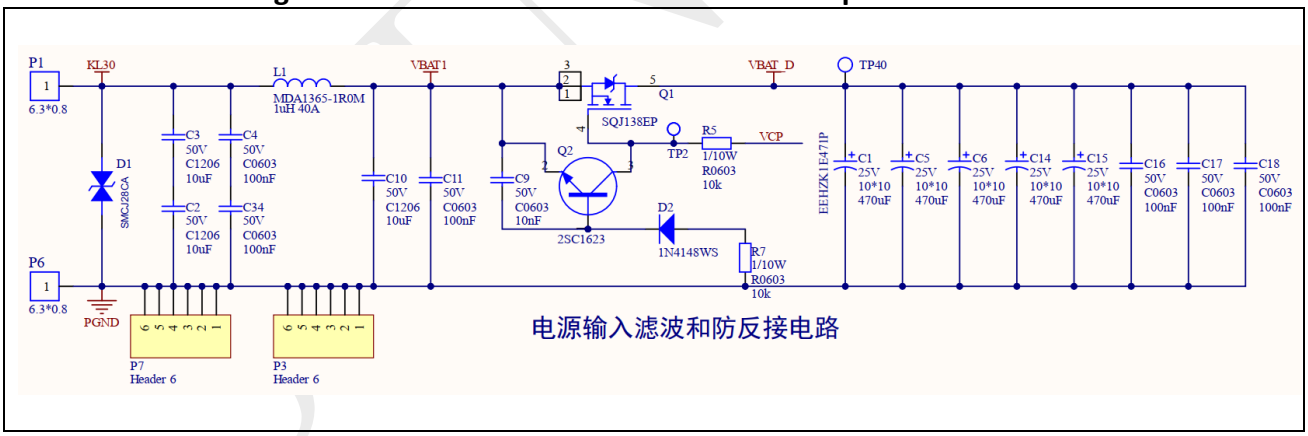
As shown in Figure 2-1, SPD1179 recommends power port input filtering circuit and high-side anti-reverse connection circuit, using the input power inductance at the entrance of the power line to do a set of CLC filtering, which can filter out the noise input to the PCB board from the power line and the noise output from the PCB board to the power line to the maximum extent.

Note:	It is best to use two capacitors in series for the KL30 input port, as there may be some high transient voltage spikes on the power line, which may form a high voltage at the input port, which will create the risk of capacitor overvoltage breakdown.

VBAT1 is powered by the chip through an independent anti-reverse diode.

VBAT1 is connected to the main power anti-reverse NMOS, VBAT_D is the mother bus voltage of the three-phase bridge, and a large capacity electrolytic capacitor is placed to provide the three-phase current for the motor operation. The G pole of the anti-reverse NMOS is directly driven by the voltage series 10k resistor of the VCP. An NPN transistor Q2 is added between the GS of the anti-reverse NMOS. When the input power output is reversed (GND is connected to 12V, KL30 is connected to 0V), R4 to D2 and then to Q2 BE will form an NPN IB conduction current, at this time Q2 will be conducting, and the high-side anti-reverse NMOS GS voltage will be clamped at about 0.3V to ensure the reliable shutdown of the anti-reverse NMOS. When the power input is normal, the NPN transistor Q2 is cut off and has no effect on the high-side anti-reverse connection circuit.

Figure 2-1 SPD1179 Recommended Power Input Filter Circuit



2.2 SPD1179 System Overvoltage Protection Policy

SPD1179 prohibits driving the three-phase bridge with an output of high power at a voltage above 28V. The recommended system working voltage range is 5.5V-16V, and the actual system software overvoltage protection point is recommended to be set at 16.2V-20V. The software detection of the bus voltage generally has a lag, and the bus voltage when the actual operation stops will be higher than the bus voltage set by the software. Therefore, you are advised to set the lowest allowable overvoltage protection value.

The hardware-implemented overvoltage protection circuit is:

A resistor divider circuit can be added to the bus voltage (VBAT_D), input to an ADC port of the chip, and then achieve accurate and fast bus overvoltage protection through the comparator inside the chip, and the protection response time can be less than 1us. It should be noted that the resistor voltage divider circuit is always connected to the bus, and a high-side switch control is needed to cut off the voltage divider circuit after the system enters the sleep mode to reduce the static power consumption of the system.

The following two overvoltage protection functions need to be configured in software:

1. The chip has an internal overvoltage and undervoltage protection (BOD) function for the VBAT voltage, which needs to be enabled in the software and configured with a reasonable overvoltage and undervoltage threshold. It is recommended to set the overvoltage threshold at 16.2V-24V, and stop the motor output after overvoltage.

2. The three-phase bridge bus voltage VBAT_D is connected to the VBATM port of the chip through an RC filter, and the voltage division circuit is integrated inside the VBATM port. This voltage can be directly detected by the ADC, that is, the VBAT_D bus voltage is measured. It is recommended that the software read the VBAT_D bus voltage in the PWM interrupt cycle and set the overvoltage threshold at 16.2V-24V, and stop the three-phase power output after overvoltage. Please refer to the PWM demo program in the software support package (SDK) to check the VBATM voltage in the PWM interrupt to realize the overvoltage protection function.

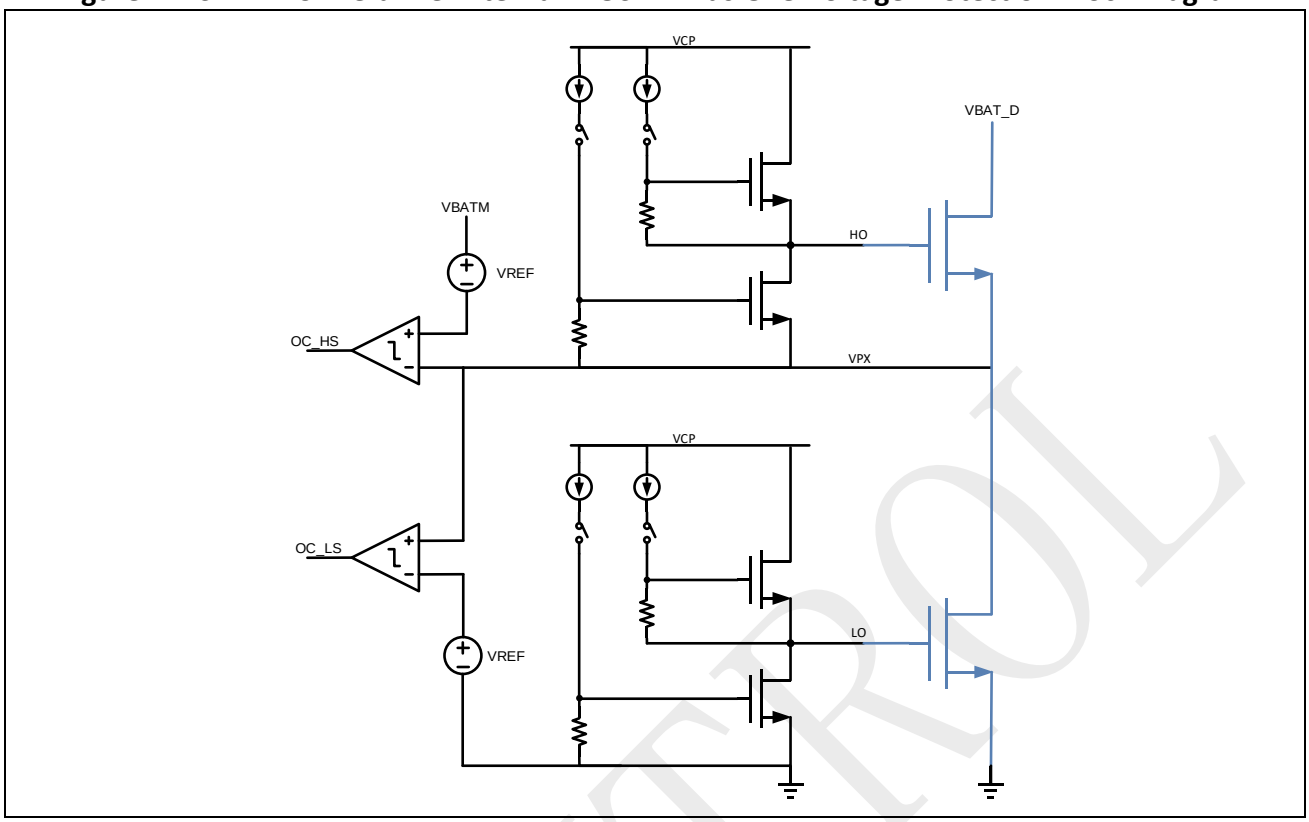
Note:	When the system is running, you need to configure the VBAT overvoltage and undervoltage protection function through software. Then the voltage of the VBATM can be queried during the PWM period to protect the bus from overvoltage and undervoltage. Finally, a voltage divider circuit with a high side switch can be added to the bus and connected to the ADC port of the chip to protect the internal comparator from overvoltage and undervoltage. For the circuit, refer to the latest DEMO schematic diagram.

2.3 SPD1179 Vds protection and sampling resistor Hardware comparator overcurrent protection

2.3.1 Setting the Vds Protection Function

Figure 2-2 below, shows six external MOSFET Vds overvoltage protection circuits (external power MOSFET overcurrent) integrated inside the SPD1179 predrive. The core of Vds protection is to detect the voltage difference between the D and S poles of the three-phase bridge MOSFET through the integrated high-speed comparator, and when this voltage difference reaches the set value and the duration exceeds the set filtering time (350ns-3.15us), the Vds protection will be triggered. This prevents the external MOSFET from being burned when a short circuit fault occurs, such as a phase short circuit or through the high side and low side bridge.

Figure 2-2 SPD1179 Pre-drive External MOSFET Vds Overvoltage Protection Block Diagram



The D-pole voltage detection point on the high side bridge is the chip VBATM pin, and the S-pole voltage detection point is each corresponding VPX pin. The D-pole voltage detection point of the low side bridge is the VPX pin corresponding to the chip, and the S-pole voltage detection point is the GND of the chip.

The configurable overvoltage threshold is 0.15V-2.4V, with a total of 16 gears, and the voltage of each gear is increased by 0.15V. There are two kinds of internal configurable filtering time, t_blank and t_filter filtering time. t_blank means that when any MOSFET of the three-phase bridge is in the switching state, some switching noise will be generated at this time, which is easy to cause Vds to trigger by mistake. Setting the t_blank time blocks Vds detection for a period of time while the MOSFET is active. The t_filter filtering time is when the Vds fault is detected and the Vds overvoltage signal of the t_filter time is continuously detected, the real Vds fault signal will be output. The t_blank and t_filter filtering time can be selected at 350ns, 750ns, 1550ns and 3150ns. For a more detailed description of protection functions, please refer to Section 27.7 of *RC-034_SPD1179 Technical Reference Manual*.

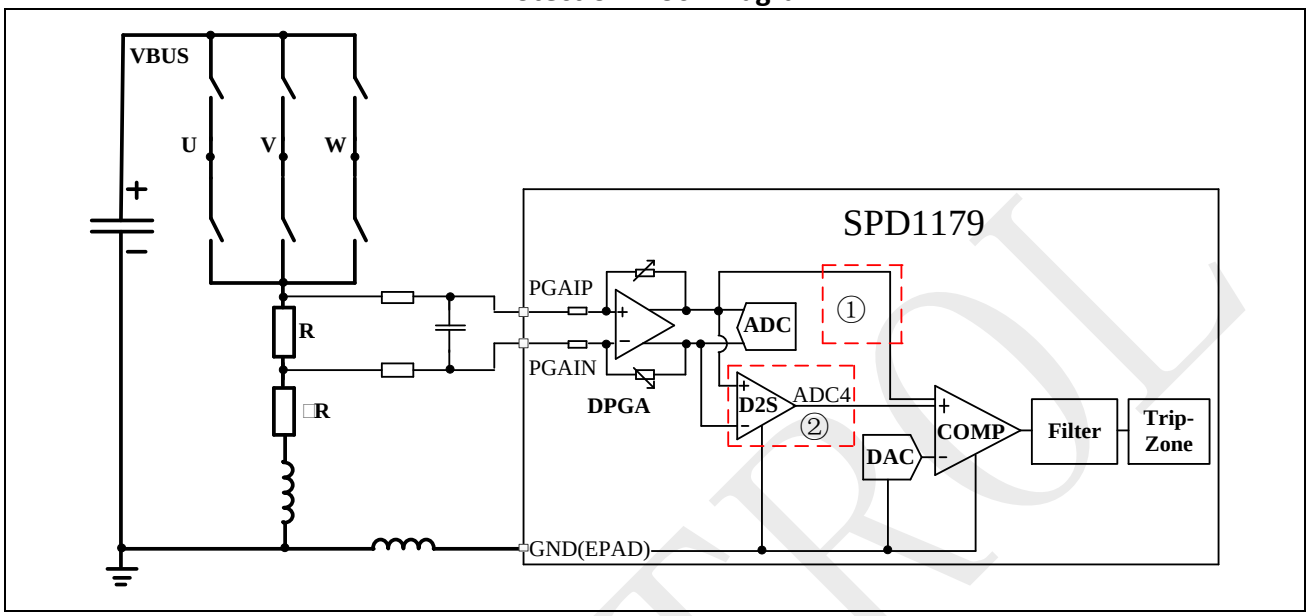
Note:	The low side bridge MOSFET Vds protection is to compare the voltage between VPX and chip GND, which will include the sampling resistor and power line voltage, so the low side bridge MOSFET Vds protection error will be large, generally will disable the low side bridge Vds protection function, the low side bridge short circuit protection can use the sampling resistor comparator overcurrent protection.

2.3.2 Sampling resistor hardware comparator overcurrent protection

As shown in Figure 2-3 below, SPD1179 differential current sampling amplifier (DPGA) can use the D2S module, DAC module and comparator module to configure the sampling resistor short-circuit

overcurrent protection function inside the chip. Through configurable comparator filtering time, it can respond to the sampling resistor overcurrent event within 1us, and then cut off the three-phase bridge output, protect power circuits from damage.

Figure 2-3 SPD1179 Sampling Resistor Configuration Comparator Hardware Overcurrent Protection Block Diagram



There are two ways to configure the internal comparator overcurrent protection.

1. The output signal of PGAIP after single-ended amplification is configured to the positive end of the comparator. Because the positive voltage of the sampling resistor is taken, it is a single-ended signal, which includes the common mode voltage generated by the negative electrode of the sampling resistor, and the overcurrent threshold will be biased. In cases where the sampling resistor value is relatively large, such as 5 milliohm, then the impact of the common-mode voltage generated by the sampling resistor negative is small, and the deviation of the protection threshold will be small. However, when the sampling resistor is 0.5 milliohm or even smaller, the common mode voltage signal generated by the negative electrode of the sampling resistor will seriously affect the setting of the protection threshold, and at this time, it is necessary to set a larger protection point or a longer filtering time to get the desired overcurrent protection point.
2. The D2S buffer integrated in the SPD1179 chip is used to subtract the differential output voltage of DPGA by using the D2S buffer to get the real voltage signals at both ends of the sampling resistor, and then sent to the positive end of the comparator for over-current comparison. The output of the D2S buffer eliminates the error caused by the common mode voltage between the lower end of the sampling resistor and the chip ground, and a more accurate overcurrent protection point is obtained.

For detailed formulas for PGAIP single-ended output and D2S buffer output voltage, please refer to Section 13 and 17 of *RC-034_SPD1179 Technical Reference Manual*.

Note:	After enabling the D2S buffer and then configuring ADC4 on the comparator, the ADC4 pin will be occupied. Make sure that the ADC4 pin is suspended and cannot be used for other functions.

In addition to the common mode voltage errors described in the above two configuration methods 1 and 2, the comparator overcurrent threshold Settings will be affected. Sampling resistor due to welding resistance value deviation, internal VDD3/2 reference voltage deviation, PGA amplification error and comparator offset voltage, DAC output voltage deviation will affect the setting of overcurrent protection point, these deviations can be collectively referred to as static deviation, static deviation can be done during the chip power-on initialization zero calibration. Because the current on the sampling resistor is zero at this time, after configuring the comparator overcurrent function, by adjusting the output result of DAC, the comparator positive voltage value (zero current value) at this time is constantly approximated (check the output result of the comparator through the register), and the software can use dichotomy to approximate, when the DAC value is consistent with the positive end of the comparator, taking the value of this DAC as the reference voltage, and setting the overcurrent point on the basis of this reference voltage, which will increase the accuracy of the setting of the protection point.

In order to improve the accuracy of the sampling resistor overcurrent comparison, it is necessary to pay attention to the PCB layout when it is best to place the bus capacitor, the sampling resistor and the chip ground point together.

2.4 Method of enabling VDD5EXT

VDD5EXT is designed as a power supply for the external sensor circuits. It is generated by the DVDD5EXT LDO, which is turned off by default, in the high voltage module. The following procedure should be followed to enable the VDD5EXT power supply:

1. Enable the high voltage module;
2. Enable the write access to the control register in the high-voltage module;
3. Enable DVDD5EXT LDO.

The reference code is as follows:

Example Code

```
/* HV Init */
HV_Init(&u16PREDRIID);

/* HV parameter write enable */
EPWR_WriteRegister(HV_REG_CTLKEY, KEY_USER_REG);

/* Enable VDD5EXT */
EPWR_WriteRegisterField(HV_REG_PMUCTL, PMUCTL_VDD5EXTEN_Msk,
PMUCTL_VDD5EXTEN_ENABLE);
```

2.5 Principle and circumvention measures of negative voltage on predrive chip pin

Figure 2-4 below shows the distribution diagram of parasitic inductance effect in a three-phase bridge.Due to the existence of these parasitic inductors, high di/dt value will be generated on these parasitic inductors when MOSFET are switched at high frequency, and high di/dt will form high transient voltage spikes on these parasitic inductors. The transient voltage spike slope can reach 1-10kV/us, or even higher, the pulse voltage amplitude can reach ±1-20V, and the duration can reach 100ns level. These transient peak voltages will first affect the MOSFET drive voltage waveform, and then the transient peak voltage (common mode voltage) will be transferred to the pin of the pre-drive chip. If the value exceeds the specified range of the chip, it will affect the function of the pre-

drive chip or even cause damage to the internal components of the chip. This needs more attention in high-power applications, or applications where the PCB power wire is very long or the loop is large due to the structure limitation, and the parasitic inductance of the power loop is large.

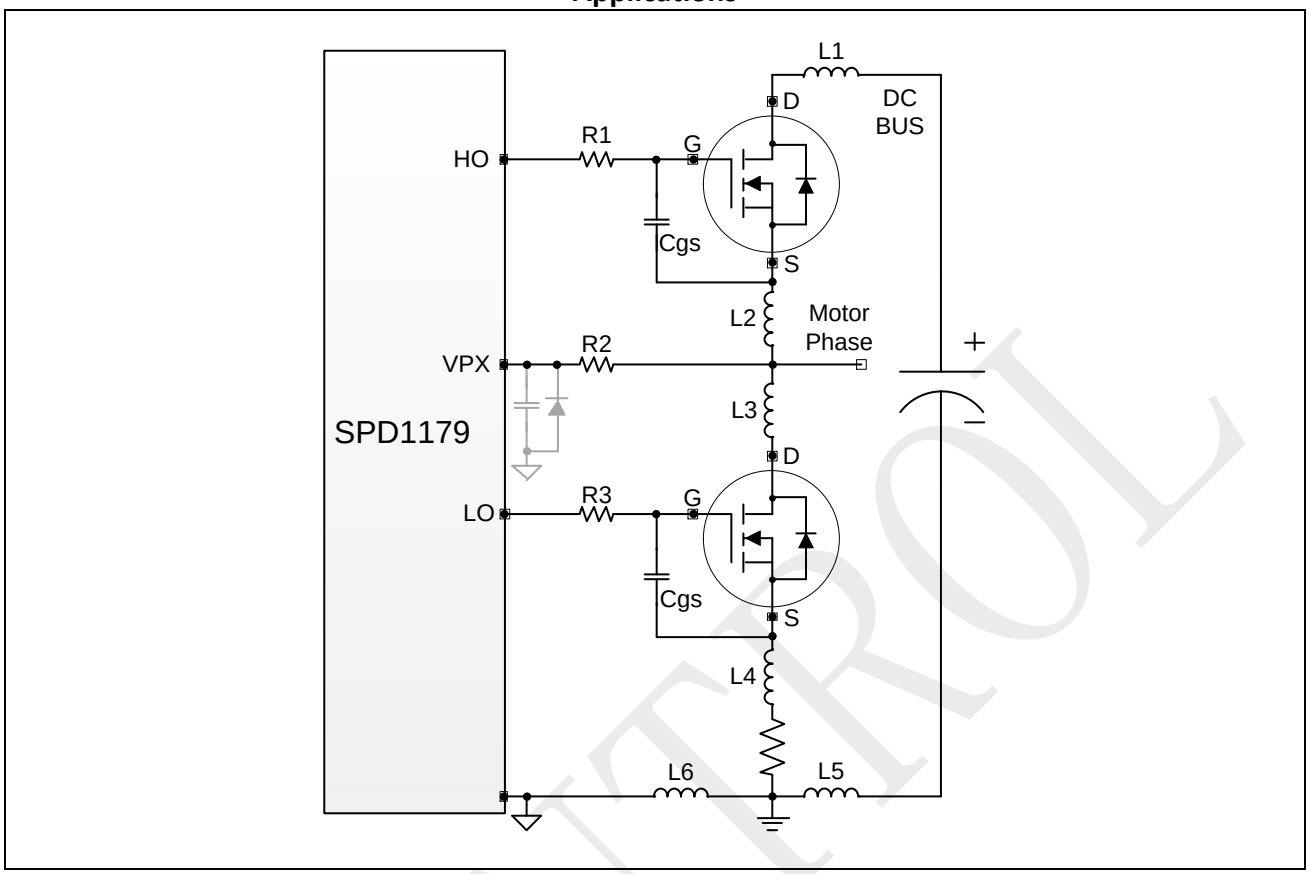
As shown in the following figure, the parasitic inductance L1 is composed of the parasitic inductance inside the high side MOSFET D pole and the parasitic inductance of the PCB power line from the high side MOSFET D pole to the positive capacitor of the bus. The parasitic inductance L2 is composed of the parasitic inductance inside the high side MOSFET S pole and the parasitic inductance from the high side MOSFET S pole to the motor connection terminal PCB. Similarly, the parasitic inductance L3 is composed of the parasitic inductance inside the low side bridge MOSFET D pole and the PCB wire from the low side bridge D pole to the motor connection terminal. The parasitic inductance L4 is composed of the parasitic inductance inside the low side bridge MOSFET S pole and the PCB line from the low side bridge MOSFET S pole to the high side end of the sampling resistor. The parasitic inductance L5 is the parasitic inductance of the PCB power line from the low side end of the sampling resistor to the negative end of the bus capacitor.

The oscillating negative voltage formed by the low side bridge MOSFET S pole due to the parasitic inductance at high di/dt will be transferred to the low side bridge drive output LO pin of the chip through the capacitor between the low side bridge GS. If the negative voltage is too large, the LO pin of the chip will be damaged. Therefore, it is recommended to increase the drive resistor R3 at the LO output, which can reduce the transient negative voltage borne by the LO pin of the chip. The recommended value of R3 is 10R-51R.

The oscillating negative voltage at the motor connection terminal and the high side bridge MOSFET S pole will be transmitted to the HO and VPX pins of the chip due to the parasitic inductance at a high di/dt. If there is too high negative voltage, the drive resistor can be increased in the output of HO and VPX to inhibit it. The recommended value range of R1 is 10R-51R. R2 can be placed around 10R according to the test situation. It is also possible to add a small capacity voltage regulator capacitor (such as 470pF) near the chip end of the VPX and perform negative voltage clamp on the switching diode at the chip site.

The oscillating voltage generated by the parasitic inductance will also affect the GS switching waveform of the MOSFET, resulting in abnormal MOSFET switching process, which needs to be tested and confirmed in the actual product.

Figure 2-4 Schematic Diagram Of Parasitic Inductance Effect Distribution In Three-phase Bridge Applications



The most effective way to reduce the parasitic inductance is to minimize the length of the PCB power line of the MOSFET S pole and the phase point at the time of PCB design. At the same time, the switching frequency of the MOSFETs should also be recuded, so the di/dt value in the loop is decreased.

3 Cautions for SPD1179 chip junction temperature calculation and actual system heat dissipation

3.1 Chip junction temperature calculation formula

The junction temperature T_J of the chip is the temperature when the transistor inside the chip is working, and it is also the place that has the highest temperature inside the chip. Measuring or calculating the junction temperature of the chip is crucial in the actual system. Limiting the junction temperature of the chip operation within the rated value can ensure the normal operation as well as the expected lifetime of the chip.

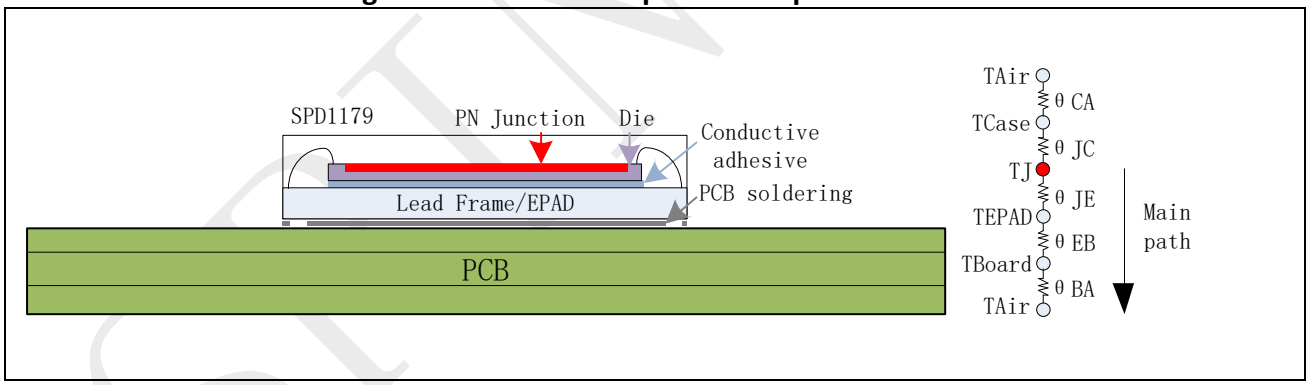
The formula for calculating or estimating the junction temperature of the chip is:

$$T_J = T_A + \theta_{JA} * P_{SPD1179} \qquad \textbf{Formula 3.1}$$

T_J is the chip junction temperature, T_A is the ambient air temperature around the chip, θ_{JA} is the thermal resistance from the chip node to the ambient air, and $P_{SPD1179}$ is the power consumption of the chip.

Figure 3-1 below shows the heat dissipation model of SPD1179 chip. The PN junction area is the heating spot of chip, and the temperature in this area is the junction temperature of chip. The junction temperature has two main heat dissipation paths, one is transmitted to the surface of the chip shell through the chip molding material, and then dissipates heat to the surrounding air through the chip shell. Another heat dissipation path is that the junction temperature is transmitted to the chip frame (EPAD) through the chip wafer, and then to the GND plane of the PCB (EPAD is welded to the PCB GND plane), and finally the heat is transmitted to the surrounding air through the PCB, which is the main heat dissipation path.

Figure 3-1 SPD1179 chip heat dissipation model



The junction temperature measurement and overtemperature protection of the chip can be carried out by using the integrated PN junction temperature sensor in the chip. The junction temperature of the chip can also be calculated by ① calculating the power consumption of the chip and ② measuring or calculating the ring thermal resistance of the system, and then the junction temperature of the chip can be calculated by using **Formula 3.1**.

3.2 SPD1179 chip power consumption calculation formula

3.2.1 VBAT Power Consumption

The internal power supply of SPD1179 VBAT adopts the cascaded LDO architecture. After the single power input from VBAT, the cascaded LDO generates 5V, 3.3V and 1.2V voltage to supply the internal module of the chip. The voltage difference between the two ends of the LDO multiplied by the LDO current is the total power consumption generated by the LDO. Therefore, the internal power

consumption of the chip can be simply estimated by calculating or measuring the average input current of the VBAT port and multiplying by the VBAT voltage.

There are two methods to obtain the current consumed by VBAT: ① See Section 5.5 of *RC-034_SPD1179 Technical Reference Manual* for the current consumption of each peripheral in the chip. Then, user can easily estimate the current consumed by the VBAT based on the chip peripherals used in the project. ② String the wire into the VBAT input pin, and then use the current indicator clamp to measure the average value of VBAT through the oscilloscope to get the VBAT consumption current, the typical value of VBAT consumption current is 40mA.

Note:	For the current consumed by VBAT, if the chip operating frequency is reduced from 100M to 24M, the current consumption will be reduced by 11.83mA. The test result of 25℃ at normal temperature is converted to an ambient temperature of 125℃, and the VBAT current will increase by 5-10mA.

3.2.2 VBATCP Partial Power Consumption

VBATCP is the input power supply of charge pump, which generates VCP voltage through two-stage charge pump, and then uses VCP voltage to generate 6 current sources to drive and control 6 MOSFETs of three-phase bridge.

VBATCP (pre-drive) part of the current consumption mainly includes two parts:

1. The current consumed by driving the external three-phase bridge MOSFETs is the same as the current consumed by charging and discharging the GS of the external three-phase bridge MOSFETs. The calculation formula is as follows:

$$I_1 = Q_{g,total} * F * 6 * 3.2 \qquad \textbf{Formula 3.2}$$

$Q_{g,total}$ is the total amount of charge required to drive one external MOSFET, including the total amount of Q_g of the MOSFET itself and the amount of charge required for the external capacitor of the MOSFET GS to be fully charged. F is the switching frequency of the three-phase bridge MOSFETs. 6 indicates that there are six external MOSFETs. 3.2 is the conversion factor, since the drive current of the current-type predrive is output from the VCP power supply, the conversion to VBATCP according to the conservation of energy should be multiplied by the coefficient of amplification, and the power consumption generated inside the chip such as charge pump control and drive control circuit are also reflected in this coefficient.

2. Pre-drive chip internal circuit power consumption.

In addition to the current required to drive the external MOSFETs, 20 mA of current is consumed by the clock and control circuits inside the predrive. When the STATIC current increases from 10mA to 100mA, the current consumed in this part will increase by about 13mA.

Note:	The STATIC current increases from 10mA to 100mA, and the VBACP consumption current increases by about 11mA. The test result of 25℃ at normal temperature is converted to 125℃ at ambient temperature, and the VBATCP current will increase by 2mA. The above values are the result of the value of VCPLVL being the SDK default value of 12V. If the VCPLVL is increased from 12V to 12.8V, the VBATCP current will increase by 5mA.

After the above analysis, the power consumption calculation formula of SPD1179 chip is as follows:

$$P_{SPD1179} = V_{VBAT} * I_{VBATCP} + V_{VBATCP} * I_{VBATCP}$$ **Formula 3.3**

3.3 Measurement and calculation of junction-to-ambient thermal resistance data

The junction-to-ambient thermal resistance represents the resistor value of disspating heat from the junction of the chip to the surrounding air (ambient), the unit is ° C /W. This value is negatively proportional to the capability of heat conduction, so a smaller value means the heat is easier to dissipate from junction to the surrounding air (ambient), in other words the junction temperature is lower when the ambient temperature remains the same.

In addition to the accurate calculation of the power consumption of the chip, the accurate calculation or measurement of the junction-to-ambient thermal resistance of the chip is also very important.

There are two methods to achieve the junction-to-ambient thermal resistance value:

1. Using The heat dissipation model of SPD1179 chip, as shown in Figure 3-1, the thermal resistance value of each part can be investigated and estimated. Then, draw the thermal resistance network from the junction to the ambient as shown in the figure, the thermal resistance value can be calculated using the series-parallel formula.
2. The junction-to-ambient thermal resistance value of SPD1179 is obtained through experiment, and the calculation formula is as follows:

$$\theta_{JA} = \frac{T_{J1} - T_{J2}}{P_1 - P_2}$$ **Formula 3.4**

θ_{JA} is the junction-to-ambient thermal resistance of the SPD1179 system, T_{J1} is the junction temperature under the condition of SPD1179 power P_1, T_{J2} is the junction temperature under the condition of SPD1179 power P_2.

The experimental method is as follows: In the real SPD1179 system environment, keep the ambient temperature constant. Then change the power of SPD1179 by increasing the voltage of VBAT and VBATCP under the same VBAT or VBATCP condition, or pulling different currents outside VDD5/VDD5EXT to change the power consumption of VBAT-VDD5/VDD5EXT LDO inside the chip. Record the junction temperature, which can be obtained through the integrated temperature sensor inside the chip, under different power. Then the θ_{JA} of the chip can be calculated using **Formula 3.4**.

The SPD1179 Datasheet gives the measured value of the junction-to-ambient thermal resistance on the test board, which is 28.0204℃/W. The PCB test board is a 110mm x 110mm x 1.6mm, two-layer board. The top layer copper coverage is 60%, the bottom layer is 80%, the copper thickness is 1oz and there is no heat radiator on EPAD.

The junction-to-ambient thermal resistance value given by the chip datasheet has special test conditions, and the vlue is completely different on a customer board. The influencing factors include: ①PCB board, PCB size, PCB layer number, PCB copper thickness and copper filling rate of each layer, the number of PCB holes, and whether the window is opened for heat dissipation. ② Whether the EPAD is connected to the entire GND plane through multiple holes, using GND plane to dissapte heat to the surrounding environment. ③ Whether the EPAD of the chip has a heat sink, the size of the heat sink, etc. Therefore, on the actual customer's application board, the junction-to-ambient thermal resistance value will be very different, and the customer needs to test the temperature rise

of the chip according to the actual situation, and then calculate the real junction-to-ambient thermal resistance of the chip.

Note:	1. The junction-to-ambient thermal resistance value given in the SPD1179 datasheet is 28.0204℃/W, but the value on the customer board is completely different, customers need to measure or calculate it in pratical. 2. For applications with very small PCB size, few PCB layers, and small copper coverage area (low power applications), the junction thermal resistance will generally be larger, so special attention should be paid to the junction temperature rise of the chip at this time. 3. Adding heat sink to dissipate the PCB ground plane connected to the chip EPAD will significantly reduce the junction thermal resistance of the chip.

3.4 Example of temperature rise calculation and measurement of SPD1179 independent-developed pump

The average input current measured on the VBAT port of the SPD1179 pump reference design (LIN communication) during full power operation (84W) is 41mA, which corresponds to the sum value of the current consumption of each module inside the chip. Under this condition, the voltage of the VBAT port is 12V, then the total power consumption inside the chip in the VBAT power field is about 12*41=492mW. The VBAT input current measurement method is to tilt the VBAT anti-reflection diode, serially connect it to a measuring wire, then measure the input current with a current clamp, and finally calculate the average value.

The measured VBATCP current of SPD1179 pump reference design is 41.86mA under full power operation, the three-phase bridge part of the pump board is configured as follows: The Qg of the MOSFET is 15nC, the external capacitor of the MOSFET GS is 2.2nF, the switching frequency of the three-phase bridge is 16kHz, the STATIC current is set to 100mA, the VCPLVL is set to 12V, and the VGSL is set to 11.4V. According to the above **Formula 3.3**, the current of VBATCP can be calculated as:

① Drive external MOSFET:(15nC+2.2nF* 12V) *16k*6*3.21=12.76mA

② Pre-drive power consumption 20mA.

③ If the STATIC value is set to 100mA, the VABTCP current consumption increases by 11mA.

The total current of VBATCP is 12.76+20+11=43.76mA. This calculated value is basically consistent with the measured value of VBATCP current, which proves the accuracy of the calculation formula. The measured value is used to calculate the final chip power consumption.

Under this condition, the voltage of the VBATCP pin is 12V, and the internal power consumption of the pre-drive part is roughly estimated to be 12*41.86=502.32mW. The current measurement method of VBATCP is to raise the series resistor, serially connect it to a measuring wire, then measure the input current with the current clamp, and finally calculate the average value.

According to the above analysis, the total internal power consumption of SPD1179 chip is the sum of the input power consumption of VBAT power supply and the output power consumption of VBATCP power supply. Based on the measured data of the pump reference design scheme, the total power consumption of SPD1179 in typical applications is 492+502.32=0.994W.

The measured steady-state junction temperature (the value of the PMU temperature sensor inside the chip) of the self-developed water pump running at full power (84W) at normal temperature (ambient temperature 26.7℃) is 69℃, and the temperature of the metal cooling housing of the water pump is 61.3℃. Compared with the ambient temperature of 26.7℃, The junction to ambient temperature rise is 42.3℃. Using the temperature rise data and the power consumption data of the chip, the junction-to-ambient thermal resistance of the independent developed pump can be reverse-derived to 42.5℃/W.

3.5 Measures to improve system heat dissipation and overtemperature protection

3.5.1 Improving the Heat dissipation of SPD1179

According to the above analysis, improving the heat dissipation of PCB is a effective way to reduce the junction-to-ambient thermal resistance of SPD1179 chip. The main ideas are as follows:

1. Enhance the heat dissipation ability of PCB board. Increase the copper full rate and copper thickness of the PCB, increase the number of holes in the PCB cooling plane, use PCB materials with high thermal conductivity, increase the number of PCB layers, PCB window opening, or increase solder and so on.
2. Chip package design and EPAD welding. For large-area EPAD, multiple holes need to be designed and connected together with the geodetic plane. During welding, EPAD and PCB should be well welded to avoid problems such as tin leakage and welding bubbles.
3. Add a heat sink to the ground plane on the back of the chip. QFN package heat dissipation is mainly through the EPAD downward heat dissipation, PCB layout will generally connect the EPAD through the hole to the earth plane, and then open a window on the ground plane of the bottom of the PCB to conduct heat into the surrounding air. When there is a radiator, add a radiator to the GND plane of the PCB for heat dissipation, which will greatly reduce the junction-to-ambient thermal resistance of the chip.
4. Reduce the operating power consumption inside the chip. Disable the module that is not used inside the chip, reduce the pre-drive current, reduce the operating frequency of the chip and other measures to reduce the power consumption of the chip.

3.5.2 Chip junction temperature measurement using MCU internal temperature sensor

SPD1179 integrates three temperature sensors, namely LIN module temperature sensor, PMU power management temperature sensor and MCU temperature sensor. These temperature sensors can be used for measuring chip junction temperature. Please refer to the examples in our SDK when using these sensors, and it is recommended to take TPMU as the reference, because the temperature at the power module is the highest.

4 Precautions for the PCB Layout of the SPD1179 chip

SPD1179 is a motor drive SOC chip with full integration, and when PCB layout is required, layout should be carefully carried out according to the chip function module. The following inspection items should be considered by customers when Layout.

4.1 Shorten the power path layout from the lower bridge S pole to the sampling resistor and then to the bus capacitor

The reference ground of the low-side bridge driving signal LO_U/V/W of SPD1179 is the GND (EPAD) of the chip, and the low-side bridge driving circuit includes the wiring from the low-side bridge S pole to the sampling resistor and then back to the GND of the chip, which has a large loop area. The wiring from the low-side bridge S pole to the sampling resistor is a power path with large current, and this path is inevitably longer due to the single resistor sampling, which will generate a larger wiring parasitic inductance. When the MOSFET switch is turned on, parasitic oscillation will be generated at the lower bridge S pole, which will affect the low-side bridge GS driving waveform and also affect the LO pin of the chip. Therefore, when PCB Layout is laid out, the length of the power path from the three-phase low-side bridge S pole to the sampling resistor and then back to the bus capacitor should be shortened as much as possible to reduce the parasitic inductance on the power path and reduce the parasitic oscillation of the low-side bridge S pole, so as to reduce the influence of the parasitic oscillation on the LO driving signal.

As shown in Figure 4-1 and Figure 4-2 below, a schematic diagram is given to shorten the length of the capacitor power path from the lower bridge S pole to the bus bar, and the schematic diagram and PCB Layout diagram of the chip ground and power ground are common at the lower end of the sampling resistor.

Note:	1. First of all, the three low-side bridge S poles should be close to each other, connected together by thick copper foil, and connected to the sampling resistor by the shortest path. Then the lower end of the sampling resistor and the GND of the bus capacitor are shared in one point. 2. The grounding point of SPD1179 digital ground and power ground is also placed at the lower end of the sampling resistor, reducing the loop area of the low-side bridge driving circuit and reducing the parasitic oscillation on the power path of the low-side bridge S pole to the LO driving signal.

Figure 4-1 Schematic diagram of shortening the line distance from the low-side bridge S pole to the sampling resistor and then to the bus capacitor

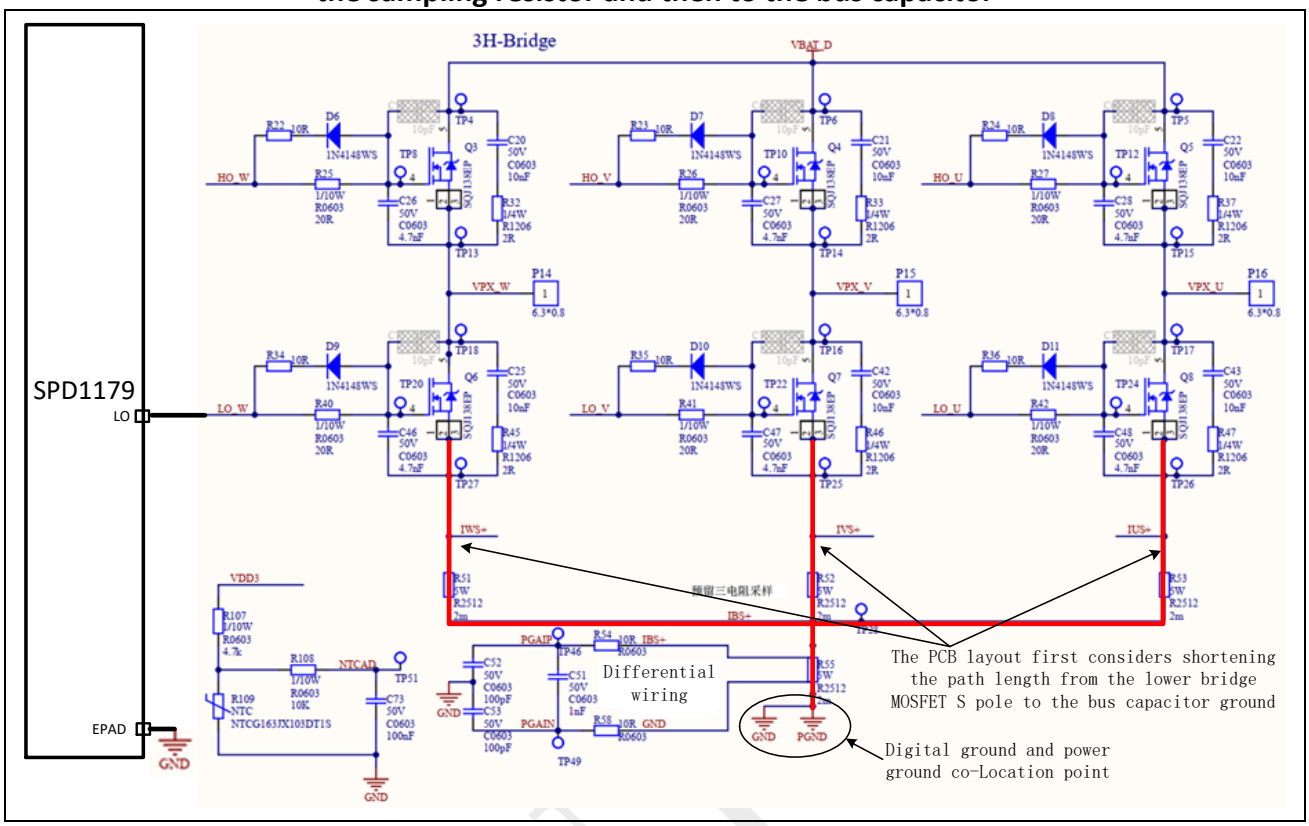
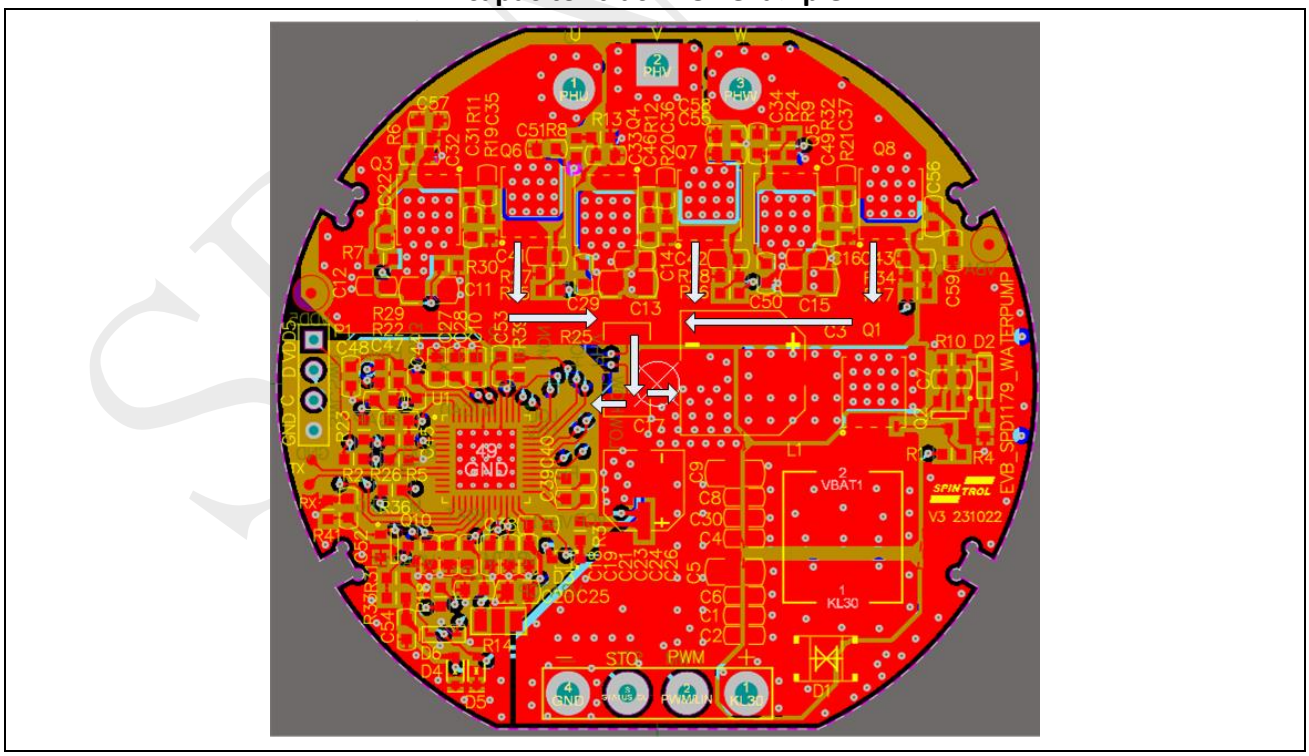


Figure 4-2 Shorten the length of the low-side bridge S pole to the sampling resistor to the bus capacitor track PCB example



4.2 Other Layout Precautions

1. The decoupling capacitor circuit around the MCU should be as short as possible, and each capacitor should have a via to the ground plane and then quickly return to the chip EPAD. This is very

critical. In PCB Layout inspection, it is necessary to check the circuit path of the chip power pin decoupling capacitor one by one. The path should be small and low impedance, mainly the capacitor returns to the chip EPAD.

2. The power supply position of VBATCP should be above the bus capacitor, not from the D pole of the MOSFET, because the voltage of the D pole of the MOSFET has a large switch oscillation voltage. Similarly, the leading position of the power supply route of VBAT should also be on the positive pole of the bus capacitor, and the power should be taken at the position where the ripple noise of the bus is small. This can significantly reduce the influence of power supply noise on the chip.

3. The power supply position of VBATM should ensure that the Vds sampling of the three-phase bridge can be accurately, it is better to take a separate sampling line, not with the VBATCP power line with the same line.

4. The capacitor between VCP and VBATCP should be close to the chip for voltage stabilization.

5. The area of the drive circuit should be as small as possible, that is, the differential line of HO_U/V/W and VPX_U/V/W, and the area of the circuit returning to the chip EPAD from the LO_U/V/W to the S pole of the low-side bridge to the sampling resistor should be as small as possible.

6. In order to ensure that the area of the low-side bridge drive circuit is as small as possible, the point where the chip ground and power ground are grounded should be placed at the lower end of the sampling resistor, and the ground of the lower end of the sampling resistor, that is, the ground of the bus capacitor, should be at the same point.

7. The area of the main power circuit should be as small as possible, and X and Y capacitors should be added to the appropriate screw connection ground position to filter.

8. Optimize the heat dissipation of the PCB as much as possible and increase the copper full rate.

9. The sampling resistor output differential line to the chip end, the filter resistor and capacitor close to the chip placement.

10. The capacitors and beads of the LIN port should be close to the chip placement.

5 Precautions for using the EMC for the SPD1179 chip

The following measures can be considered in advance, either inside the chip or at the beginning of the design, to ensure that the system passes EMC testing.

5.1 LIN communication EMC countermeasures

LIN communication mainly affects low-band noise (500k-10M), and the dv/dt of the rising and falling edge of LIN signal can be adjusted through the integrated emission slope control function in the SPD1179 LIN module to improve the low-band radiation noise. LIN communication needs to add 220pF capacitor near the chip port, and LIN needs to series magnetic beads near the chip end, and the magnetic beads need to have a certain impedance in the low frequency band such as @1M. The recommended magnetic bead model is MMZ1608B102CT or BLM18HE152SN1D. LIN communication requires the addition of magnetic beads near the chip in order to pass the BCI 200mA level test.

5.2 SPD1179 Internal spread frequency Function

The frequency of the internal charge pump of SPD1179 is 312kHz, and when the charge pump expansion frequency is enabled, the charge pump frequency jumps between 156kHz and 312kHz. The latest software support package (SDK) has defaulted to always enable charge pump expansion frequency for better passing of EMC high-frequency noise radiation tests.

The clock frequency of the internal charge pump of the chip is 40MHz (5V), which provides the time reference for current-type pre-drive regulation, as well as filtering time setting for Vds protection. The internal 40M clock draws high-frequency currents from the VDD5 power supply, which can easily cause EMC radiation problems with 40M and its frequency multiplier terms. Therefore, in PCB design, it is necessary to ensure that the loop impedance of the VDD5 de-coupling capacitor from positive to VDD5 pin and from negative to EPAD is as small as possible. At the same time, the VDD5 power supply should not be external power supply, do not lengthen the wire, and the VDD5 cable should be far away from the edge of the board to reduce the antenna effect. At the same time, the software can implement the 40MHz clock spread function to help radiate noise through the 40MHz clock and its multiple frequency band.

5.3 Adjust the power MOSFET switching speed to resolve high-frequency noise

Generally, the high-frequency noise in motor control systems is caused by dv/dt and di/dt of the three-phase bridge MOSFET switch. For example, 30MHz noise is caused by conduction current radiation. The determination method can be confirmed by comparison tests such as the difference between high power and low power, motor operation without load and 50% duty cycle wave comparison test to determine whether it is related to the action of the three-phase bridge MOSFET switch. When the Qg of some MOSFETs is very small, the possibility of high-frequency noise caused by MOSFETs is greater, and at this time, the switching speed of MOSFETs can be reduced by increasing the drive resistance or increasing the GS capacitance, or even the GD capacitance, or reducing the drive capability of the current-type drive, to pass the conduction radiation test. An appropriate RC absorption circuit can also be added between the DS of MOSFETs.

5.4 Grounding of the motor stator or metal shell

Generally, the three-phase PWM voltage signal of the motor control system will form an antenna to radiate low-frequency noise to space through the motor winding, and the noise frequency is about 150k in the radiation low frequency band. Dealing with such low-frequency switching frequency radiation noise can reduce such spatial radiation by placing the motor stator through the measure of connecting the capacitor to the PCB board ground, or the measure of connecting the motor iron shell to the PCB ground plane to release the noise and low impedance of the low-frequency radiation generated by the motor stator line to the ground plane.

5.5 Other EMC Information

Adjusting the static current of the pre-drive will also affect the results of the BCI experiment, especially when some MOSFETs are selected with low turn-on voltage, such as Vgs (th) about 1V. when the high-frequency noise is injected into the positive and negative lines of the power supply in BCI, the high-frequency noise will be injected into the G pole of the MOSFET through the GD capacitance of the MOSFET, which will affect the GS voltage of the MOSFET, possibly causing the GS voltage of the MOSFET to rise, resulting in mis-turn-on problem. At this time, by increasing the GS capacitance or increasing the internal static current of the chip, the MOSFET GS voltage can be stabilized, so as to avoid the bus current fluctuation, or the Vds voltage misprotection and other problems.

6 Precautions for welding SPD1179 chips

SPD1179 adopts the mainstream wetable flank QFN package form of current automotive electronic chip, which exposes the cutting position of the flank pin of the standard QFN package through plating process, the flank is plated with tin. At this time, when soldering, the tin will climb to the side of the QFN package pin, forming an arc tin climbing. In this way, the tin climbing state of the chip side can be checked by AOI optical detection, and then the reliability of soldering can be checked to improve the reliability of production.

If the customer has not touched the chip before, please pay attention to the confirmation and adjustment of the process parameters during welding, which involves the production of the chip package graphics, the production of the chip steel mesh graphics, the selection of solder and the curve setting of the welding furnace temperature. Please refer to *The SPD1179 Wettable Flank QFN Package Welding Guide*.

In addition to confirming the reliability of soldering through AOI optical detection, internal impedance and diode measurement parameters of SPD1179 are provided, as shown in Table 6-1 and Table 6-2. By measuring the impedance at the on-board test points and the diode characteristics of the chip, the reliability of the chip's soldering can be further validated. It is strongly recommended that customers perform impedance and diode characteristic measurements after chip soldering to ensure the reliability.

Table 6-1 SPD1179 Internal Resistance Measurement Table

Items	Pin name	Normal chip（Ω）
Resistance (The red positive probe should be connected to the pin being measured, and the black negative probe should be connected to GND or the other end.) Note: When there is a resistor or capacitor connected next to the Pin, the resistance characteristics will deviate from the reference values.	VBAT	OL
	VBATCP	OL
	VBATM	OL
	VCP	OL
	CFBOT0	OL
	CFBOT1	OL
	CFTOP0	OL
	CFTOP1	OL
	OUTH_U/V/W-VPX_U/V/W	65k/65k/65k
	OUTH_U/V/W - VCP	OL/OL/OL
	VPX_U/V/W	171k/171k/171k
	OUTL_U/V/W-GND	65K/65K/65K
	VCP-VPX_U/V/W	OL/OL/OL
	VDD5	126k-400k
	VDD5_EXT	2.5M
	VDD33	600k
	MON	OL
	LIN	OL

Table 6-2 SPD1179 Diode Characteristics Measurement Table

Items	Pin name	Normal chip（V）

Diodes (The red positive probe should be connected to GND or the front end, and the black negative probe should be connected to the rear end.)	GND to VCP	0.55
	GND to VBATCP	0.55
	GND to VBATM	0.55
	GND to CFTOP0	0.61
	GND to CFTOP1	0.61
	GND to CFBOT0	0.61
	GND to CFBOT1	0.61
	VBATCP to CFTOP0	0.722
	CFTOP0 to CFTOP1	0.725
	CFTOP1 to VCP	0.722
	VBATCP to VCP	0.733
	VPX_U/V/W to VCP	0.693/0.693/0.693
	GND to LIN	OL
	GND to MON	OL
	GND to GPIO2	0.544
	GND to OUTL_U/V/W	0.634/0.634/0.634
	GND to VBAT	0.559
	GND to VDD5EXT	0.535
	GND to VDD5	0.495
	GND to VDD33	0.492
	GND to VCAP12	0.377