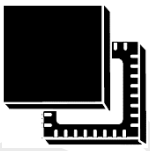
SPD1179/SPD1176 Datasheet

32-bit ARM® Cortex-M4F based auto-grade MCU with LDO, integrated 2-phase/3-phase pre-driver with supply up to 28V

Features

- 32-bit ARM® Cortex-M4F CPU with FPU
  - 100 MHz maximum frequency
- Memories
  - Up to 128 KB embedded flash
  - Up to 1 KB emulated EEPROM
  - Up to 32 KB on-chip SRAM
- Power Management
  - Single battery supply from 5.5V to 28V (42V for load dump).
  - Integrated 3.3V and 5V LDO for MCU and main I/O supply
  - Integrated 5V LDO for external sensor
  - Sleep mode and stop mode for power saving
  - POR, Brown-out detector (BOD)
- Pre-Driver Module
  - 2-Phase/3-Phase Pre-Driver for motor control
  - Integrated charge pump for 100% duty cycle
  - Programmable driving capability up to 290mA
  - Programmable output swing from 8V to 11V
  - Four/Six external power FET V_{DS} monitors
- Clock
  - Crystal oscillator with both internal oscillator and external clock input support
  - Internal 32MHz factory-trimmed oscillator
  - Internal 32MHz backup-safety oscillator
  - PLL for CPU clock, maximum up to 100MHz
- 8-channel DMA controller



QFN48 (7 x 7 mm, 0.5mm pitch)
QFN56 (8 x 8 mm, 0.5mm pitch)

- 13-bit A/D converter (up to 9 channels)
  - As low as 200 ns conversion time
  - Single-ended and differential sampling
  - Open/short detection for safety
- Three temperature sensor
  - 1 x T-sensor for MCU
  - 1 x T-sensor for PMU
  - 1 x T-sensor for LIN transceiver
- Monitoring ADC (13-bit)
  - Monitor critical voltages
- Programmable gain amplifier (PGA)
  - One single-ended PGA with gain option:
    1, 2, 4, 8, 16, 32, 48, 64
  - One differential PGA with gain option:
    2, 4, 8, 16, 24, 32, 48, 64
  - Differential PGA supports -1.5V ~+2V input
- Analog comparator
  - Two (one pair) high-speed comparators with digital deglitch filter
- Integrated phase voltage comparison
  - 3-phase voltage sensing and 1-reference sensing
  - 3 dedicate phase comparator
- Three 10-bit DACs and 1 DAC buffer
- One D2S (Differential to single-ended) buffer

- LIN transceiver compatible with LIN spec 2.2A and SAEJ2602-2
- 1 input with high voltage monitoring
- PWM
  - Four enhanced PWM modules
  - 8 PWM outputs in total
  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 27 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Up to 9 GPIO with 3.3V
  - Up to 18 GPIO with 5V
  - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and APWM mode selection
- Debug mode
  - Serial wire (SW) debug & JTAG interfaces
- 6 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - Sy stick timer 24-bit down-counter
- Communication interfaces
  - UART (with LIN support) x 2, An external LIN PHY required for UART1
  - SPI x 2
  - I2C x 1
  - CAN (with FDCAN support) x 1
- Security Modules
  - 64-bit unique ID, CRC x 1
- Operating temperature
  - SPD1179
    Junction temperature: -40 to +150°C.
    Ambient temperature: -40 to +125°C.
    Automotive AEC-Q100 Grade 1 class
  - SPD1176
    Junction temperature: -40 to +125°C.
    Ambient temperature: -40 to +105°C.
    Industrial grade

Table 1-1: SPD1179/SPD1176 device features and peripheral counts

Peripheral	SPD1179DPW48	SPD1179ZDPW48	SPD1179YDPW48	SPD1179XDPW48	SPD1179YDPW56	SPD1179XDPW56	SPD1179DPW56	SPD1176APW48	SPD1176ZAPW48	SPD1176APW56
Flash (KB)	128	64	64	128	64	128	128	128	64	128
Emulated EEPROM (KB)	1									
SRAM (KB)	32	16	16	32	16	32	32	32	16	32
DMA (8-channel)	1									
3.3V GPIOs	5				9	9	9	5		9
5V GPIO	14				18	18	18	14		18
13-bit ADC	1									
Number of analog input channels	5				9	9	9	5		9
Single-ended PGA	1									
Differential PGA	1									

Peripheral	SPD1179DPW48	SPD1179ZDPW48	SPD1179YDPW48	SPD1179XDPW48	SPD1179YDPW56	SPD1179XDPW56	SPD1179DPW56	SPD1176APW48	SPD1176ZAPW48	SPD1176APW56
Analog comparators	2									
Phase comparators	3									
DAC	3									
PWM	4									
Number of overall PWM channels	8	8	8	8	8	8	8	8	8	8
Number of PWM channels internally connected to pre-driver	6	6	6	6	6	6	6	6	6	6
ECAP	1									
General-purpose timers	3									
Watchdog timers	2									
CRC	1									
CAN	1									
UART	2									
SPI	2									
I2C	1									
Pre-driver	3-phase		2-phase				3-phase			
LIN Transceiver	1 (connected with UART1 internally)									
Maximum CPU frequency (MHz)	100MHz									
Junction temperature	-40 ~ +150 °C							-40 ~ +125 °C		
Grade	Automotive (AEC-Q100 Grade-1)							Industrial		

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Revision history

Revision	Date	Author	Status	Changes
1	03-Mar-2021	H. Huang	Outdated	Initial release.
2	17-Apr-2021	H. Huang	Outdated	1. Modifies description of D1~D6 Conditions in Table 5-32: LIN transmitter characteristics. 2. Update DPGA common mode input range in Section 2.28 and Table 5-22: DPGA characteristics. 3. Update Figure 3-1: SPD1179(Z)/SPD1176 QFN48 pinout.
3	22-Oct-2021	H. Huang	Outdated	1. Update Features. 2. Add Section 2.30. 3. Update symbols in Table 5-22: DPGA characteristics and Table 5-23: SPGA characteristics.
4	06-Jan-2022	H. Huang	Outdated	1. Update Table 5-22: DPGA characteristics, add DPGA settling time for all gain configurations. 2. Add annotation for LIN transceiver characteristic in Section 5.21. 3. Update Figure 3-1: SPD1179(Z)/SPD1176 QFN48 pinout, modify the description for debug pins and HV power pins. 4. Add D2S buffer information and characteristics. 5. Table 5-15: (VCP – VBAT) BOD characteristics. 6. Update Figure 3-1: SPD1179(Z)/SPD1176 QFN48 pinout, change AVGND to AGND. 7. Update Section 2.17. 8. Add Figure 1-2: SPD1179/SPD1176 application diagram. 9. Update features of Pre-Driver module.
5	7-Jun-2022	H. Huang	Outdated	1. Update Table 5-8: Peripheral current consumption. 2. Update 3. Figure 5-2: Typical operational current versus frequency. 4. Update Table 5-2: Recommended operating conditions. 5. Update Table 5-3: 5V IO Electrical characteristics (VDVDD5 = 5V). 6. Update **Table** 5-4: 3.3V IO Electrical characteristics (V_{DVDD33} = 3.3V). 7. Update Section 5.4.

Revision	Date	Author	Status	Changes
				8. Update Table 5-24: Analog comparator characteristics.
6	8-Jul-2022	H. Huang	Outdated	1. Update Conditions of parameter R_{PU} and R_{PD} in Table 5-3: 5V IO Electrical characteristics (VDVDD5 = 5V). 2. Update Table 5-4: 3.3V IO Electrical characteristics (VDVDD33 = 3.3V). 3. Update VBATM Pin description in Table 3-1: SPD1179/SPD1176 QFN48 pin definitions.
7	28-Jul-2022	H. Huang	Outdated	1. Update Features. 2. Update Figure 1-1: SPD1179/SPD1176 block diagram and Figure 1-3: Clock tree. 3. Add Section 2.23, Section 2.35 and Section –. 4. Update Table 3-1: SPD1179/SPD1176 QFN48 pin definitions. 5. Add Section 3.2 and Section 6.2 for QFN56 package. 6. Update Figure 4-1: Memory map. 7. Update Table 7-1: Ordering information.
A/0	17-Qct-2022	H. Huang	Outdated	1. Update document format. 2. Add Section 3.3. 3. Update Figure 1-1: SPD1179/SPD1176 block diagram and Figure 1-3: Clock tree. 4. Update Figure 4-1: Memory map. 5. Update Table 5-20: Monitoring ADC characteristics.
A/1	20-Nov-2022	H. Huang	Outdated	1. Update Figure 3-1, Figure 3-3, Table 3-1 and Table 3-2, Rename Pin ‘AGND’ to ‘GND’. 2. Update Table 5-40: ESD absolute maximum ratings. 3. Update Figure 4-1, add EPWR memory mapping. 4. Update Features, add operating temperature information for SPD1176. 5. Update junction temperature T_J for SPD1176 in Table 5-1 and Table 5-2. 6. Update Section 6.1, modify the information of QFN48 package.
A/2	05-Dec-2022	H. Huang	Outdated	1. Update Figure 1-1, Rename ’13-bit FuSa ADC’ to ’13-bit Monitoring ADC’. 2. Update Section 2.16, update the ADC information for monitoring power. 3. Update the notes for BOOT pin usage. 4. Update Section 2.24, add SPI FIFO depth information. 5. Update Table 3-1 and Table 3-2, modify the

Revision	Date	Author	Status	Changes
				description of DVDD5 pin. 6. Update Figure 4-1, add memory mapping for Dedicated 1KB EEPROM Emulation. 7. Add Table 1-1: SPD1179/SPD1176 device features and peripheral counts. 8. Update Section 2.25, add notes for CAN wake-up function. 9. Update Ordering Number.
A/3	05-Jan-2023	H. Huang	Outdated	1. Update Table 1-1, add SPD1179X / SPD1179Y / SPD1179Z device features and peripheral counts. 2. Add Figure 3-2: SPD1179X/SPD1179Y QFN48 pinout. 3. Update Table 3-1, modify the pin description of PIN29 ~ PIN31. 4. Update Table 7-1, add ordering information for SPD1179X / SPD1179Y / SPD1179Z.
A/4	09-Jan-2023	H. Huang	Outdated	1. Update Table 5-22: DPGA characteristics, add GBW and SR parameter values.
A/5	16-Jan-2023	H. Huang	Outdated	1. Update the notes of Figure 3-2: SPD1179X/SPD1179Y QFN48 pinout.
A/6	04-Feb-2023	H. Su	Outdated	1. Update Table 5-43: Thermal resistance characteristics, modify the measurement parameter
A/7	11-Feb-2023	H. Su	Outdated	1. Update Table 1-1: SPD1179/SPD1176 device features and peripheral counts, add peripheral. 2. Update Table 7-1: Ordering information, add peripheral.
A/8	23-Feb-2023	W. Han A. Li C. Hu	Outdated	1. Update Section 5.4. 2. Update Section 5.1. Add the absolute maximum rating for V_{LIN}, V_{MON} and V_{LIN_GND} in Table 5-1. 3. Rename RCO0 to RCO. 4. Rename RCO1 to ROSC. 5. Update peripheral current consumption. 6. Update typical current consumption. 7. Update SPI module clock limitation to 100MHz, not 50MHz. 8. Update Table 5-22, update common mode input range value. 9. Update Section 2.28. Change “Wide common mode input range: -0.5V ~ 2V” to “Wide common mode input range: -1.5V ~ 2V”. 10. Update voltage range description in Section 1, Section 2.8, Section –, Section 5.2,

Revision	Date	Author	Status	Changes
				Section 5.6, Section 5.20, Section 5.21, Section 0, Section 5.24, Section 0, Section 5.26 and Section 5.27. 11. Update IO characteristic in Section 5.3. 12. Update test requirement in Section 5.8, Section 5.10 and Section 5.11. 13. Add phase comparator characteristic in Section 5.16. 14. Add current consumption in Section 5.4. 15. Add frequency variation with temperature in Section 5.7. 16. Update feature description. 17. Update DVDD33 BOD characteristic in Section 5.6. 18. Update CAN module description in Section 2.25. 19. Update the operating supply voltage range from 5.5V to 28V. Delete the internal supply voltage range description in Chapter 5 for DVDD5 and DVDD33. 20. Update the symbol name documentation type in Chapter 5. 21. Update the description of temperature sensor in Section 2.27 and add the temperature sensor characteristic in Section 5.12. 22. Re-order sections in Chapter 2 and Chapter 5. 23. Add description on the rule of ordering number in Chapter 7.
A/9	14-Apr-2023	C. Hu	Outdated	1. Update Section 5.4. 2. Update Section5.5, add pre-driver condition in active mode for current consumption. 3. Update Table 5-3 and Table 5-4. 4. Add Section 5.30 Moisture Sensitivity Level.
A/10	23-May-2023	C. Hu	Outdated	1. Update Table 5-34. 2. Update Section 2.11. 3. Update Table 5-1. 4. Update Table 5-16 5. Update Table 5-19, Table 5-20, and Table 5-22. 6. Update Table 7-1. 7. Update Table 5-19. 8. Update Table 5-29. 9. Update Section 2.2.

Revision	Date	Author	Status	Changes
A/11	10-Jul-2023	C. Hu	Outdated	1. Update Table 1-1. 2. Update Chapter 1. 3. Update Figure 6-3, Figure 6-4 and Table 6-2.
A/12	10-Aug-2023	C. Hu	Outdated	1. Add Figure 5-1: Cold power-up transition time. 2. Update Table 5-1, change the absolute maximum rating of V_{VCP} and V_{OUTH} to 48V. Add the note for maximum ramp-up rate of power supply. 3. Update Table 3-1 and Table 3-2, change the absolute maximum rating of V_{VCP} to 48V. 4. Update Table 5-19 and Table 5-20, change the gain error over temperature is +/-40LSB.
A/13	21-Nov-2023	C. Hu	Outdated	1. Update Table 5-1, add the maximum range value for V_{VCP} - V_{VBATCP} as 15.8V. 2. Update Table 5-15, update the detected voltage by BOD is V_{VCP} - V_{VBAT}. 3. Update Figure 1-2, update pre-driver and charge-pump circuit and decoupling cap for LDO. Add the input filter circuit for supply. 4. Update Table 7-1, add the order information for SPD1179XPW56 and update the description for the grade of product. 5. Update Table 1-1, add the product information for SPD1179XPW56. 6. Update Section 2.11 and Figure 2-1 for the description of wake-up for stop mode. 7. Update Table 5-29, add the electrical characteristic of threshold for drain vs source voltage monitor.
A/14	6-Dec-2023	C. Hu	Outdated	1. Change the annotation of Table 5-31, the minimum filter time of LIN wake-up is 100us. 2. Change the annotation of Table 5-34, the minimum filter time of MON wake-up is 50us. 3. Change the minimum capacitor load as 2.2uF in Table 5-35. 4. Change the minimum capacitor load as 2.2uF in Table 5-36. 5. Update T_{slope} and T_{offset} in Table 5-21. 6. Update Figure 1-2. Update capacitor as 2.2uF for DVDD5 to GND and update the capacitor as 2.2uF for DVDD33 to GND.
A/15	2024-03-14	C. Hu	Outdated	1. Update Table 1-1 and Table 7-1, add the product and order information for SPD1179XPW56. Add pinout information in

Revision	Date	Author	Status	Changes
				Figure 3-4 and update the pin information in Table 3-2. 2. Correct the typo error of annotation and update the specification of D5 and D6 in Table 5-32. 3. Update Figure 1-2. Update capacitor as 4.7uF for DVDD33 to GND and update the capacitor as 2.2uF for VCAP12 to GND. Change fly across capacitor from 100nF to 220nF. 4. Update Table 3-1 and Table 3-2. Fix the capacitor as 4.7uF for DVDD33 to GND. 5. Update the specification of gain error and offset in Table 5-22. 6. Update the specification of gain error and offset in Table 5-23. 7. Update the lowest limitation as 0.475*V_{VBAT} for LIN wake-up threshold in Table 5-31.
C/0	2024-07-25	Jiali.Zhou	Released	1. Delete the UART compatibility statement for ISO 16550A and 16750 in Section 2.22，since the register map is not compatible. 2. Update Table 5-1, add time to SPD1179 for continuous operation at 150°C junction temperature. 3. In Table 3-1, add extra 0.1uF capacitor for pin20, change capacitance from 100nF to 220nF for pin 25~28. 4. In Table 3-2, change capacitance from 100nF to 220nF for pin 31~34. 5. Fix typo for conditions for I_{PU} and I_{PD} in Table 5-34, typical value of V_{out} in Table 5-35, Table 5-36, Table 5-37. Add drive capabilities in Table 5-35. 6. Update DVDD5EXT, VBATCP-VCP capacitance and voltage values in Figure 1-2. 7. Update Document Styles. 8. Update Table 5-1 note 7，modify the maximum allowable power-up slope of the VBAT from 1V/us to 0.1V/us.

Terms or abbreviations

Terms or abbreviations	Description
BEMF	Back Electro-Motive Force
DPGA	Differential Programmable Gain Amplifier
SPGA	Single-ended Programmable Gain Amplifier
D2S	Differential to Single-ended

1 Device overview

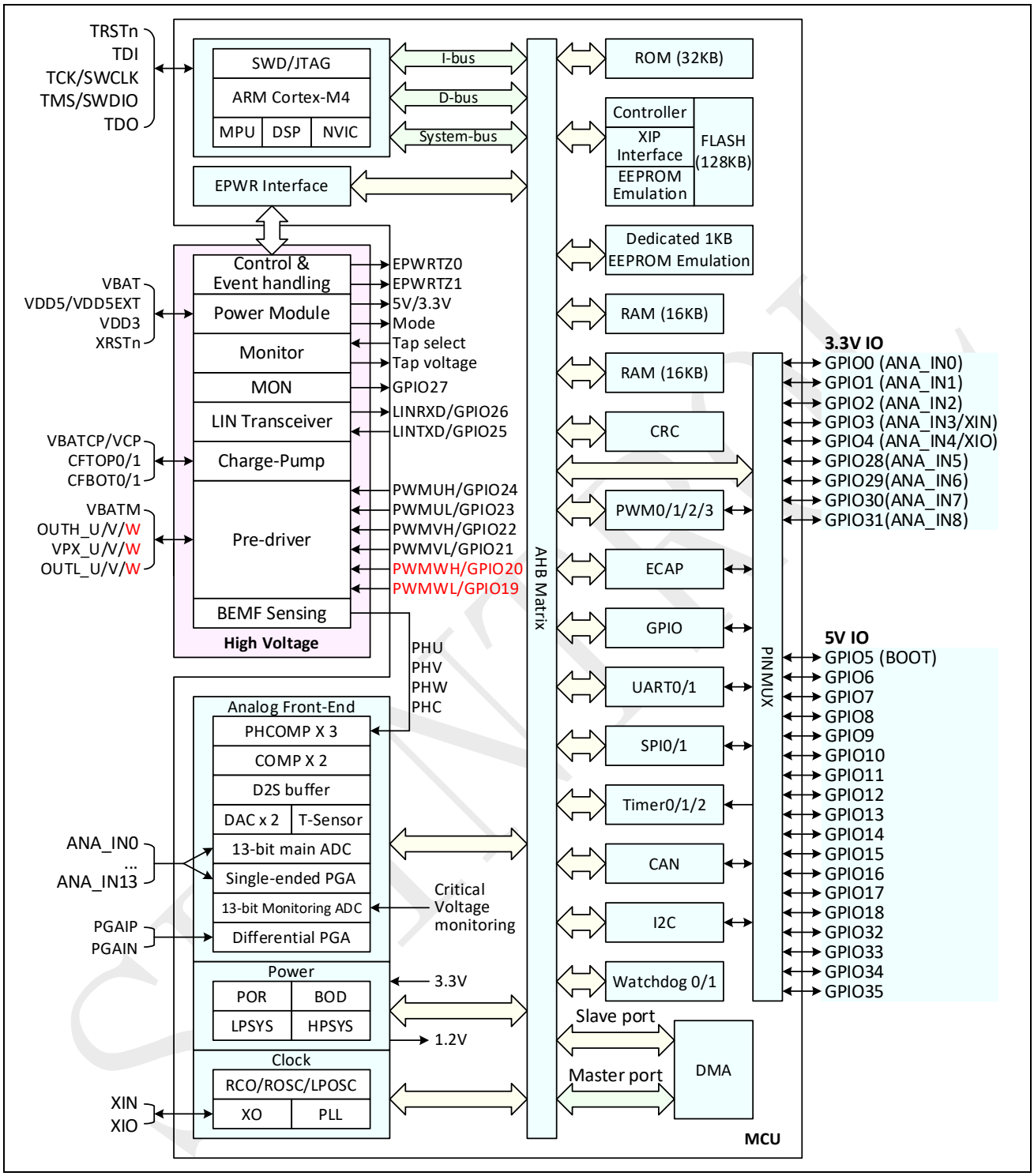
The SPD1179 device from Spintrol is a highly integrated system-on-chip (SoC) microcontroller. The SPD1179/SPD1176 incorporates a 32-bit ARM® Cortex-M4F high-performance processor with a software-programmable clock rate up to 100 MHz, 32 KB SRAM, 128 KB embedded flash with up to 1 KB EEPROM emulated by extra 12 KB flash, and an extensive range of enhanced I/Os and peripherals. The device offers a 13-bit ADC, one differential PGA and one single-ended PGA, four enhanced PWMs, three general-purpose 32-bit timers, as well as standard and advanced communication interface: two UARTs with LIN support, two SPIs, one I2C and one CAN.

The SPD1179/SPD1176 operates with a single power supply from 5.5V to 28V (42V for load dump) and supports stop/sleep mode for power saving. It integrates two 5V LDOs for internal power system and external sensor, and also integrates 3.3V and 1.2V LDOs for MCU operation. It supports 5V I/O for logic and 3.3V I/O for analog input channel. The junction temperature range is from -40 ^{o}C to +150 ^{o}C. The package type is 48-pin or 56-pin wettable flank QFN.

The SPD1179/SPD1176 employs function safety features such as backup clocking scheme, watchdog timer interrupt and reset, open/short detection and background critical voltage monitoring. All these features make the SPD1179/SPD1176 ideal for motor control in automotive application.

Figure 1-1 shows the functional block diagram for the SPD1179/SPD1176. Figure 1-2 shows the application diagram. Figure 1-3 shows the clock tree information.

Figure 1-1: SPD1179/SPD1176 block diagram



[1] The W-phase control signals of the Pre-driver are not applicable for SPD1179X/ SPD1179Y.

Figure 1-2: SPD1179/SPD1176 application diagram

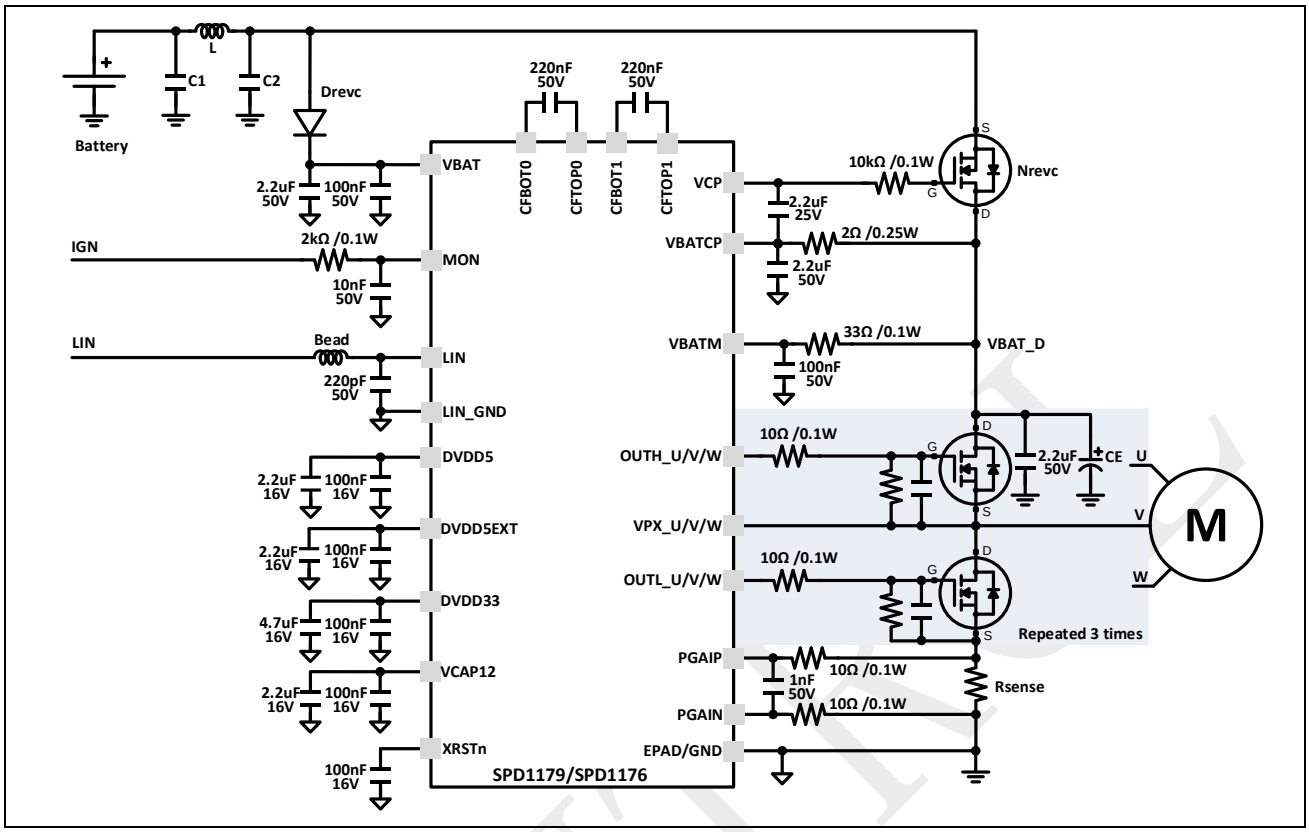
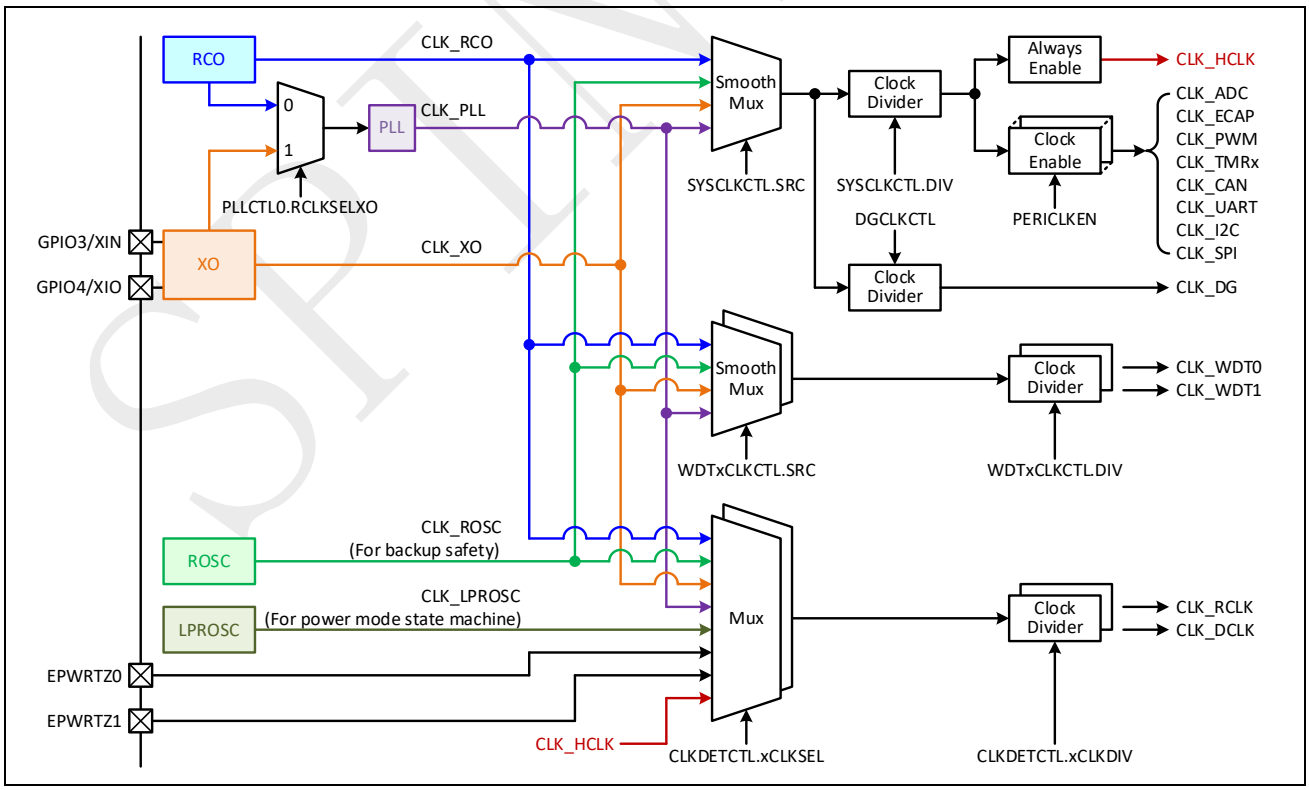


Figure 1-3: Clock tree



2 Feature descriptions

2.1 ARM® Cortex-M4F core

The ARM® Cortex-M4F processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPD1179/SPD1176 integrates a full-feature ARM® Cortex-M4F core that can run up to 100MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Serial wire and JTAG debug port (SWJ-DP)

The embedded ARM® SWJ-DP interface is combined by JTAG and serial wire debug port. They are connected to the external I/O port as shown in Table 2-1. The debug port can be disabled when enabling SPD1179/SPD1176 certain security feature.

Table 2-1: Debug interface definition

Pin Name	Serial wire mode (Disable SWV)	Serial wire mode (Enable SWV)	JTAG mode
GPIO15	User specified function channel	User specified function channel	TDI
GPIO16	User specified function channel	SWV	TDO
GPIO17	SWD	SWD	TMS
GPIO18	SWCK	SWCK	TCK

[1] The purpose of setting GPIO16 through the 24th bit of ARM® Cortex-M4F register (CoreDebug->DEMCR) located at address 0xE000EDFC: 1—SWV output; 0—function specified by user through software.

Note: In debug mode, TRSTn must be tied to the logic high(5V).

2.3 Boot ROM

The Boot ROM contains boot code, Flash software library code and emulated EEPROM software library code. User can call these software library to access the Flash memory and the emulated EEPROM directly.

2.4 Embedded SRAM

The SPD1179/SPD1176 has implemented 32 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock frequency with 0 wait states.

2.5 Embedded Flash memory

Up to 128 KB of embedded Flash memory is available for storing programs and data. To enhance the lifetime and store critical data, another 12 KB Flash memory is used for EEPROM emulation to support up to 1 KB effective capacity.

2.6 Nested vectored interrupt controller (NVIC)

The SPD1179/SPD1176 embeds a nested vectored interrupt controller able to handle up to 54 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M4F) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.7 External interrupt/event controller

The SPD1179/SPD1176 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.8 Power supply and Reset

The SPD1179/SPD1176 supports single power supply (VBAT) from 5.5V to 28V, which powers internal voltage regulators, analog circuitry on chip and the IOs. In addition, for 42V supply, chip will survive for load dump. There are no special power-up sequence requirements for the SPD1179/SPD1176.

The SPD1179/SPD1176 supports 5V I/O capability for GPIO5 ~ GPIO18/GPIO32 ~ GPIO35 and 3.3V I/O capability for GPIO0 ~ GPIO4//GPIO28 ~ GPIO31.

The SPD1179/SPD1176 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.9 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the power supply and different domain power (VBAT/DVDD5/DVDD5EXT/DVDD33/VCAP12) and compare them to the programmable threshold. An interrupt or reset can be generated when voltage of the power domain is above the up-boundary or below the low-boundary. The interrupt service routine then generates a warning message and/or put the MCU into a safe state.

2.10 Clocks

System clock selection is performed on startup. The internal 32 MHz factory-trimmed oscillator is selected by default upon reset. External crystal with frequency from 4MHz to 32MHz can be attached to GPIO3 and GPIO4, so as to generate high precision clock using on-chip crystal oscillation circuits. User can also directly use external clock via GPIO3.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal 32MHz oscillator or external clock as the input reference. The output frequency covers from 25MHz to 100MHz.

Several clock dividers allow the configuration of the AHB, and the peripherals frequency. The maximum allowed frequency is 100MHz. See Figure 1-3 for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 32MHz backup-safety oscillator makes the SPD1179/SPD1176 get rid of clock stuck.

2.11 Power management unit

The power management unit generates all the required supplies for the embedded MCU (DVDD5, DVDD33, VCAP12) and external supply (VDD5EXT). The power management system ensures safe behavior of SPD1179/SPD1176, and has a state machine to control power modes transition. The SPD1179/SPD1176 has implemented the power management module with following features:

- Support three power modes (active, stop and sleep)
  - ➢ Active mode

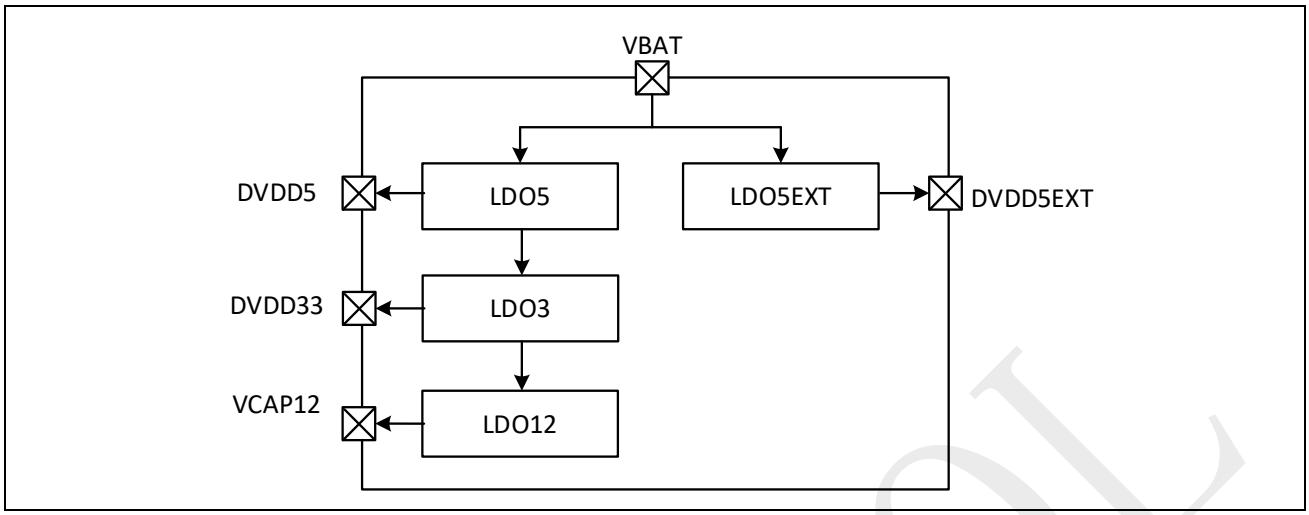
    The voltage regulators (DVDD5, DVDD33, VCAP12) are supplied by on-chip LDO with full current driving capability. All clocks are enabled per user's setup in register control bits.
  - ➢ Stop mode

    All clocks are stopped except for the 100 KHz clock for power mode state machine. DVDD5, DVDD33, VCAP12 are supplied by low-power LDO with limited current driving capability. VCAP12 can be configured to be below 1.2V to further reduce the static current. All registers and memories retain the content. The system can be waken-up by different wake-up sources, like XRSTn, LIN, MON, cyclic-wakeup and cyclic-sense-wakeup by any GPIO per user's setup with programmable input levels. The CPU will continue to run the instructions when it exit stop mode (XRSTn wake-up will trigger system reset).
  - ➢ Sleep mode

    The voltage regulators (DVDD5, DVDD33, VCAP12) are totally shutdown. It can be waken-up by LIN/MON/cyclic-wakeup and the whole system will go through a cold start-up.
- The voltage regulators (DVDD5, DVDD33, VCAP12 and VDD5EXT) supports over-current, over/under-voltage protection
- Provide over-temperature protection
- Configurable wakeup sources (LIN, MON, cyclic wakeup, cyclic sense wakeup, GPIOs)

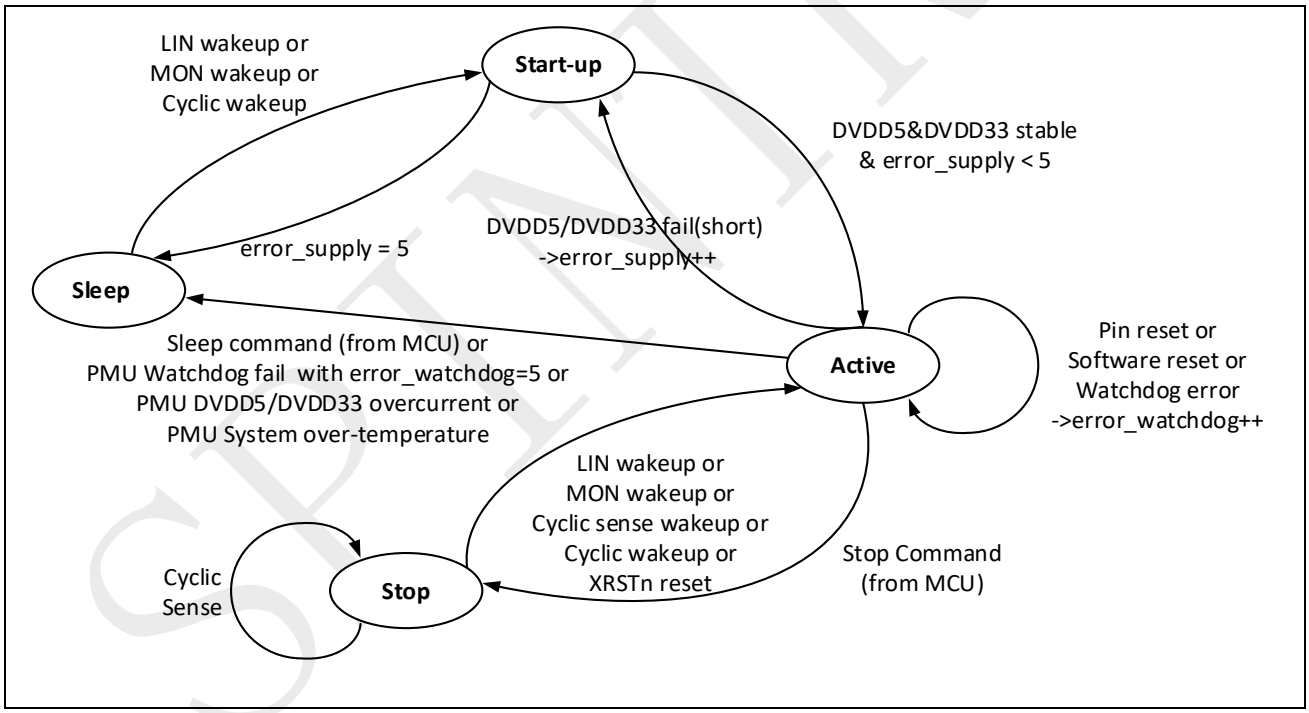
The power system diagram is shown in Figure 2-1.

Figure 2-1: Power management unit



The three power modes transition is shown in Figure 2-2.

Figure 2-2: Power modes transition



2.12 DVDD5 LDO

The DVDD5 LDO provides power for 5V domain functions. The SPD1179/SPD1176 has implemented a DVDD5 LDO module with following features:

- 5V LDO with 80mA driving ability
- Overcurrent monitoring and self-shutdown
- Pre-regulator for DVDD33 LDO
- Pull down current source (typically 5mA) at the output for sleep mode only

2.13 DVDD33 LDO

The DVDD33 LDO provides power for 3.3V domain functions. The SPD1179/SPD1176 has implemented a DVDD33 LDO module with following features:

- 3.3V LDO with 50mA driving ability
- Overcurrent monitoring and self-shutdown
- Pre-regulator for VCAP12 LDO
- Pull down current source (typically 100uA) at the output for sleep mode only

2.14 DVDD5EXT LDO

The DVDD5EXT LDO provides power for external circuits. The SPD1179/SPD1176 has implemented a DVDD5EXT LDO module with following features:

- 5V LDO with 40mA driving ability
- Overcurrent monitoring and self-shutdown
- Pull down current source(typically 100uA) at the output for sleep mode only

2.15 VCAP12 LDO

The VCAP12 LDO provides power for the embedded MCU. The SPD1179/SPD1176 has implemented a VCAP12 LDO module with following features:

- 1.2V LDO with 40mA driving ability

2.16 Power tracking amplifier

Power tracking amplifier buffers critical power signals to the 13-bit Monitoring ADC, to monitor power status. The critical power signals sent to the 13-bit Monitoring ADC are VBAT, VCP, VMON, VDD5, power bandgap, PMU temperature sensor voltage and LIN temperature sensor voltage.

2.17 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM.

- If GPIO5 is high upon power-on reset, XRSTn pin reset or the system reset request from the ARM® Cortex-M4F, ISP boot mode is entered. The boot loader reprograms the embedded Flash by using UART or LIN interface. When UART interface is used, GPIO10 is configured as UART0_TXD and the GPIO11 is configured as UART0_RXD.
- For all other cases, the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000.

2.18 General-purpose IOs (GPIOs)

The SPD1179/SPD1176 can be configured to support as many as 27 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter
- Pure 3.3V I/O capability multiplexed with ADC input channel for GPIO0~GPIO4, GPIO28 ~ GPIO31
- Full 5V I/O capability for GPIO5 ~ GPIO18, GPIO32 ~ GPIO35

2.19 General Purpose Timers

The SPD1179/SPD1176 includes three identical general-purpose timers, which features:

- Independent clock enable control
- 32-bit auto-reload down-counter
- Generate interrupt request, ADCSOC event and PWMSYNC event when the counter reaches zero
- Support 4 modes
  - General timer: Periodic down-counter
  - Gated timer: Down-counter enabled by external input level
  - Event counter: Down-counter upon external input edge
  - Event capture: Down-counter with timestamp latched upon external input edge

2.20 Watchdog timer

The SPD1179/SPD1176 implements two identical watchdogs, which features:

- Independent clock source, clock dividing and clock enable control
- 32-bit auto-reload down-counter
- Generate interrupt request when the counter reaches zero
- Generate reset request when the counter reaches zero and the interrupt flag is already set
- Can be frozen or free-running in debug mode

2.21 SysTick timer

There is a SysTick timer embedded in the ARM® Cortex-M4F. It is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter with auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.22 UART

The SPD1179/SPD1176 has two UART modules. They features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5 – 8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 6.25 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

Specific hardware is also implemented to enable LIN features:

- Compatibility with LIN 1.3, 2.0, 2.1 and 2.2A protocols
- Configurable baud rate up to 20 kbps
- Identification masks for message filtering
- Hardware processing on break field, sync byte field, protected ID field, data field and checksum field
- Response length can be defined by bit 5 and bit 4 of protected ID field, or by register control
- Programmable classic checksum mode or enhanced checksum mode

2.23 I^2C

The I^2C bus interface complies with the common I^2C protocol and can operate in standard mode (with data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s). It features:

- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.24 SPI

SPD1179/SPD1176 includes two SPI modules, which allow half/full-duplex, synchronous, serial communication with external devices. They features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- Local clock divider for flexible communication speed control, with up to 50 Mbps capability
- MSB-first data order
- Programmable clock polarity and phase
- 16 x 32-bit deep transmit and receive FIFOs, respectively

2.25 CAN

The SPD1179/SPD1176 has implemented one CAN module. It is used for communication based on CAN protocol. An external CAN transceiver is required for the connection to the physical layer (CAN bus). The CAN module features:

- Compatible with ISO-11898-1:2015 specification, whose frame format is called classical CAN and ISO-FDCAN.
- Compatible with Bosch CAN2.0B specification.
- Compatible with Bosch FDCAN V1.0 specification, whose frame format is called NONISO-FDCAN.
- Support Bus-Off recovery.
- Support automatic message re-transmission after transmission failure.
- Support restricted mode.
- Support monitor mode.
- Support test mode.
- Support 64 mailboxes with independent message identifier mask for each mailbox.
- Support automatic remote frame handling.
- Support CAN bus error recording.
- Support 32-bit timestamp.

Note: The CAN module of SPD1179/SPD1176 does not support wake-up function, users need to select a CAN PHY that supports wake-up function and connect the CAN PHY wake-up signal to the MON pin or GPIO pin of SPD1179/SPD1176 to realize the CAN wake-up function.

2.26 ADC

One 13-bit analog-to-digital convert is embedded into SPD1179/SPD1176 and has up to nine external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has built-in sample-and-hold (S/H) with two input channels, which is suitable for differential sampling. The start of sample and conversion can be triggered by the software, the internally connected hardware event signals from the general-purpose timers and the PWM outputs, or from the external pin input.

The 13-bit ADC features:

- 200 ns minimum conversion time and independent configurable sampling time
- Support single-ended or differential sampling
- Full range analog input: 0 V to 3.65 V
- Input open and short detection for safety

Another 13-bit ADC (Monitoring ADC) is provided to routinely check critical voltages below per user's request for system safety concern. An interrupt can be generated if the monitoring item is out of the pre-defined range.

Please see Table 5-19 for 13-bit ADC characteristics and Table 5-20 for Monitoring ADC characteristics.

2.27 Temperature sensor

SPD1179/SPD1176 includes three temperature sensors. One for MCU, one for PMU in high voltage and one for LIN transceiver. Their sensing voltages vary linearly with temperature. These sensing signals are internally connected to the input channel of monitoring ADC, which is used to convert the sensor output voltage into a digital value.

2.28 PGAs

SPD1179/SPD1176 includes a differential programmable gain amplifier (DPGA) with two dedicated pins. It features:

- Programmable gains: 2, 4, 8, 16, 24, 32, 48 and 64
- Differential input voltage: ±2.7/PGA_Gain
- Wide common mode input range: -1.5V ~ 2V with Gain 2x
- Settling time: 250 ns to 1.4 us

A single-ended PGA (SPGA) is also implemented in SPD1179/SPD1176. The four external ADC input channels (ANA_IN0~ANA_IN3), the temperature sensor output, and internal 1.2V power can be selected as the SPGA input. It features:

- Programmable gains: 1, 2, 4, 8, 16, 32, 48 and 64
- Settling time: 300 ns to 2 us

Both the outputs from the differential PGA (DPGA) and the single-ended PGA (SPGA) can be selected as the 13-bit ADC input. Please see Table 5-22 for DPGA characteristics and Table 5-23 for SPGA characteristics.

2.29 Analog comparators

The SPD1179/SPD1176 has two high-speed comparators. They are used with two internal 10-bit DAC as reference for monitoring PGA inputs or outputs to check whether the voltage is too high or too low. The comparator output is routed to the PWM Trip-Zone modules.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter

Please see Table 5-24 and Table 5-26 for analog comparator and DAC characteristics.

2.30 Phase comparators

SPD1179/SPD1176 include 3 high speed rail-to-rail phase comparators, which can compare three phases voltage (PHU/PHV/PHW) to the common mode voltage (PHC). Phase comparator has 8-to-1 input mux, it can also used as normal comparator to compare analog ADC input to reference voltage (ADC input or DAC output).

Based on the intrinsic characteristic of motor operation, hardware post-processing is implemented to the comparator output as below, so as to simplify user's software.

- Blanking with programmable window size
- Filtering with programmable window size
- Finite state machine (FSM) to ignore the systematic false alarm due to the large interferences via motor toggling. The FSM can be reset to initial state per user's software. The first zero-crossing event after the FSM reset is ignored.

2.31 DAC and DAC buffer

The SPD1179/SPD1176 has three 10-bit DAC, which can generate a voltage from 0 to VDDA. DAC0 and DAC1 can be used as too high or too low reference for comparators. DAC2 can be used as the reference of phase comparator.

The SPD1179/SPD1176 has one DAC buffer, it can select DAC0 or DAC1 as its input, and send output through ANA_IN2 pin.

2.32 D2S buffer

The SPD1179/SPD1176 integrates one D2S (differential to single-ended) buffer, which can convert DPGA's differential output voltage to single-ended output voltage and sent it to ANA_IN4 pin. Through external RC filter (typically, R = 1kΩ, C = 1uF), the single-ended output voltage can be sent back to ANA_INx (x = 0 ~ 3) pin and measured by 13-bit ADC. D2S buffer gain is fixed at 0.5.

2.33 PWMs

The SPD1179/SPD1176 integrates four PWM modules and supports six PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.34 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPD1179/SPD1176 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.35 Cyclic redundancy check (CRC)

The SPD1179/SPD1176 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Eight CRC standard polynomials supported

2.36 Pre-Driver System

Pre-Driver system consists of a two/three low-side and high-side pre-drivers which can drive the two/three phases of low-side and high-side external power NFET's. The SPD1179/SPD1176 has implemented this Pre-Driver system with following features:

- Embedded dual charge pump guarantees 100% duty cycle
- High performance down to 5.5V supply
- Built in non-overlap time to prevent craw-bar current even in case of input PWM overlapping
- Dynamically adjustable Pre-Driver charge/discharge strength to optimize switching and EMI

- VDS monitors for short circuit detection in on- and off-state

2.37 LIN transceiver

The local interconnect network (LIN) module is a serial communication protocol designed to support automotive networks in conjunction with controller area network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The SPD1179/SPD1176 has implemented an LIN module (connected to UART1 internally) with following features:

- Operational with VBAT 7.0 to 18 V DC, functional up to 28 V and down to 5.5V. For load dump, VBAT can survive up to 42V.
- Support 2 transmission modes 10.4kBaud/20kBaud, functional download with 115.2kBaud
- Integrated 30kΩ termination resistor for slave applications
- Compatible with LIN protocol specification 2.2, and SAEJ2602-2
- Low standby current in Sleep mode
- Over-temperature protection
- TxD timeout feature (optional, enabled by default)
- Very high immunity against electromagnetic interference

2.38 High voltage monitor

The high voltage monitor (MON) module is dedicated to monitor external high voltage levels above or below a specified threshold (normally is VBAT/2). Its output can be used as an digital level from high voltage pin or used to detect a wake-up event at the high-voltage MON pin in low-power mode.

The SPD1179/SPD1176 has implemented an MON module with following features:

- High voltage input with VBAT/2 threshold voltage
- Integrated pull-up and pull-down current sources with automatic selectable capability
- Wake-up event for power saving modes
- Level shift from high voltage pin to low voltage domain

2.39 BEMF sensing

The back electromotive force (BEMF) sensing module is used to detect zero crossing events, which can be used as a commutation trigger for BLDC applications.

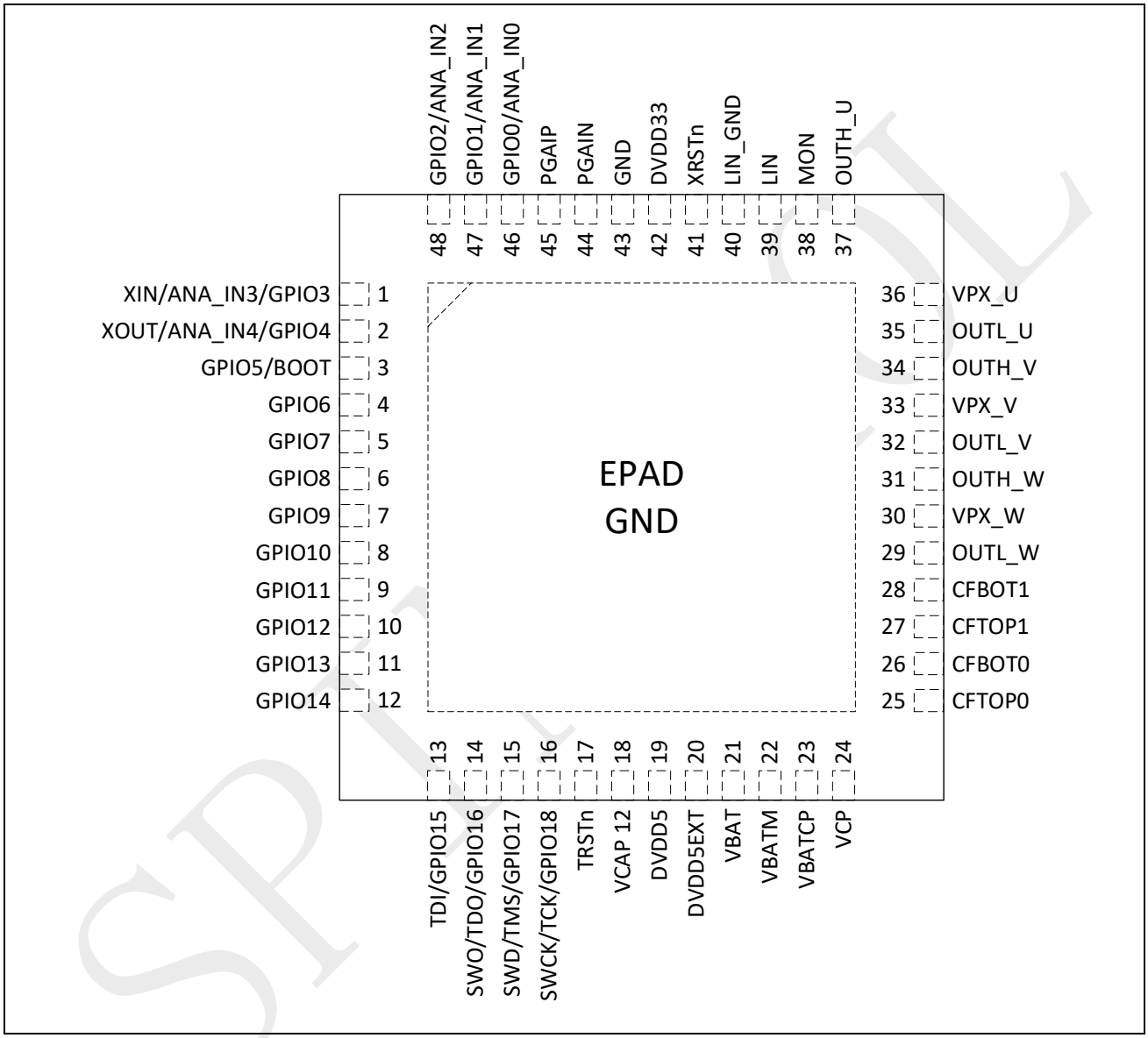
The SPD1179/SPD1176 has implemented a BEMF sensing module with following features:

- Implement U/V/W phase zero crossing detect
- BEMF detection scheme with the virtual neutral point

3 Pinout and pin description

3.1 QFN48

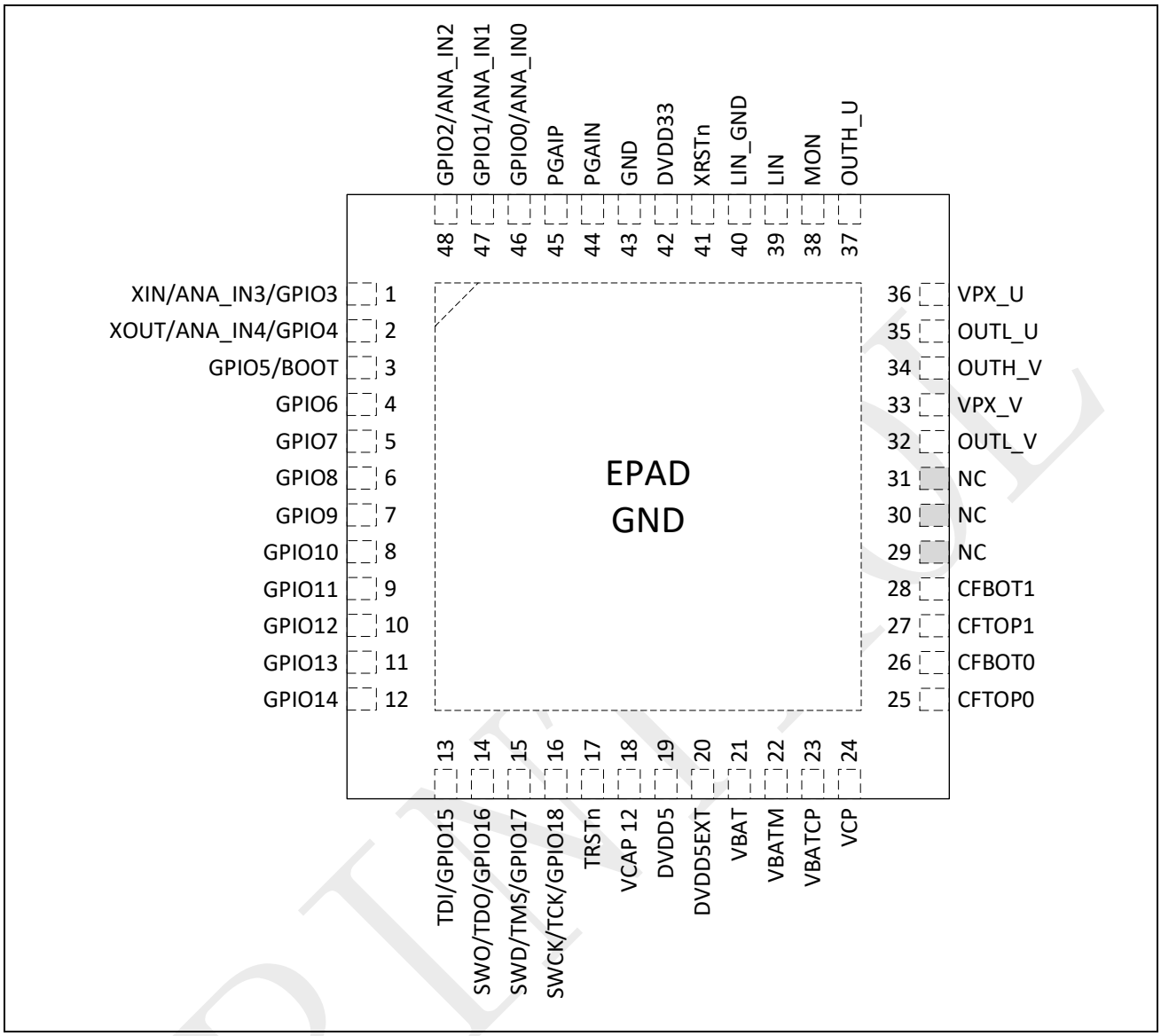
Figure 3-1: SPD1179(Z)/SPD1176 QFN48 pinout



[1] The figure above shows top view for the package.

[2] When TRSTn is high, GPIO15 ~ GPIO18 may be used for debug interface as shown in Table 2-1.

Figure 3-2: SPD1179X/SPD1179Y QFN48 pinout



[1] The figure above shows top view for the package.

[2] When TRSTn is high, GPIO15 ~ GPIO18 may be used for debug interface as shown in Table 2-1.

Table 3-1: SPD1179/SPD1176 QFN48 pin definitions

Pin	Type	Signal	Sub-Type[1]	Description
1	3.3V I/O	GPIO3	I/O	General-purpose input/output 3
		ANA_IN3	AI	Analog input channel 3
		XIN	AI	External oscillator input
		COMP_MON0	O	Comparator output monitor 0
2	3.3V I/O	GPIO4	I/O	General-purpose input/output 4
		ANA_IN4	AI	Analog input channel 4
		XOUT	O	External oscillator output
		COMP_MON1	O	Comparator output monitor 1
3	5V I/O	GPIO5 (BOOT)	I/O	General-purpose input/output 5 (BOOT)
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZ0O or EPWRTZ1O.

		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		ECAP_APWMO	O	APWM mode output of the ECAP
4	5V I/O	GPIO6	I/O	General-purpose input/output 6
		SPI0_SCLK	I/O	SPI0 clock input/output
		UART1_TXD	O	UART1 transmitted data
		COMP_MON2	O	Comparator output monitor 2
5	5V I/O	GPIO7	I/O	General-purpose input/output 7
		SPI0_SFRM	I/O	SPI0 frame signal input/output
		UART1_RXD	I	UART1 received data
		COMP_MON3	O	Comparator output monitor 3
6	5V I/O	GPIO8	I/O	General-purpose input/output 8
		SPI0_MOSI	I/O	SPI0 master output, slave input
		CAN_TXD	I/O	SPI0 master input, slave output
		COMP_MON4	O	Comparator output monitor 4
7	5V I/O	GPIO9	I/O	General-purpose input/output 9
		SPI0_MISO	I/O	SPI0 master input, slave output
		CAN_RXD	I/O	SPI0 master output, slave input
		COMP_MON5	O	Comparator output monitor 5
8	5V I/O	GPIO10	I/O	General-purpose input/output 10
		UART0_TXD	O	UART0 transmitted data
		PWM0A	O	PWM0 output A
		I2C_SCL	I/O	I2C clock
9	5V I/O	GPIO11	I/O	General-purpose input/output 11
		UART0_RXD	I	UART0 received data
		PWM0B	O	PWM0 output B
		I2C_SDA	I/O	I2C data
10	5V I/O	GPIO12	I/O	General-purpose input/output 12
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWM1A	O	PWM1 output A
		PWM3A	O	PWM3 output A
11	5V I/O	GPIO13	I/O	General-purpose input/output 13
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWM1B	O	PWM1 output B
		PWM3B	O	PWM3 output B
12	5V I/O	GPIO14	I/O	General-purpose input/output 14
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWM2A	O	PWM2 output A
		I2C_SCL	I/O	I2C clock
13	5V I/O	GPIO15	I/O	General-purpose input/output 15
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWM2B	O	PWM2 output B
		I2C_SDA	I/O	I2C data
		TDI	I	JTAG data input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
14	5V I/O	GPIO16	I/O	General-purpose input/output 16

		UART1_TXD	O	UART1 transmitted data
		CAN_TXD	O	CAN transmitted data
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		TDO/SWO	O	JTAG data output or Asynchronous TRACE output
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
15	5V I/O	GPIO17	I/O	General-purpose input/output 17
		UART1_RXD	I	UART1 received data
		CAN_RXD	I	CAN received data
		SPI1_SCLK	I/O	SPI1 clock input/output
		TMS/SWD	I/O	JTAG mode select or SWD data
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
16	5V I/O	GPIO18	I/O	General-purpose input/output 18
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		PWMSYNCO	O	PWMSYNC output
		ECAP_APWMO	O	APWM mode output of the ECAP
		TCK/SWCK	I	JTAG clock or SWD clock
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
17	5V I/O	TRSTn	I	JTAG reset pin, reset the JTAG when low
18	1.2V Power	VCAP12	P	1.2 V power **Add 2.2uF and 0.1uF bypass ceramic cap to GND**
19	5V Power	DVDD5	P	5 V digital power **Add 2.2uF and 0.1uF bypass ceramic cap to GND**
20	5V Power	DVDD5EXT	P	5 V power for external loading **Add 2.2uF and 0.1uF bypass ceramic cap to GND**
21	HV Power	VBAT	P	High voltage power from 5.5V to 42V **Add 2.2uF and 0.1uF bypass ceramic cap to GND**
22	HV Power	VBATM	P	High voltage power for vds monitor from 5.5V to 42V **Add 0.1uF bypass ceramic cap to GND. Series 33 Ohm resistor from VBAT_D (VBAT for driver).**
23	HV Power	VBATCP	P	High voltage power for charge-pump from 5.5V to 42V **Add 2.2uF bypass ceramic cap to GND. Series 2 Ohm resistor from VBAT_D (VBAT for driver).**
24	HV Power	VCP	P	Charge-pump output voltage, maximum up to 48V. **Add 2.2uF ceramic cap to VBAT_D (VBAT for driver).**

25	HV Power	CFTOP0	P	Charge pump flying capacitor 0 top plate voltage **Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0**
26	HV Power	CFBOT0	P	Charge pump flying capacitor 0 bottom plate voltage **Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0**
27	HV Power	CFTOP1	P	Charge pump flying capacitor 1 top plate voltage **Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1**
28	HV Power	CFBOT1	P	Charge pump flying capacitor 1 bottom plate voltage **Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1**
29	HV IO	OUTL_W	O	Pre-Driver W-Phase low side FET gate drive **Only applicable in SPD1179(Z)/SPD1176**
	-	NC	-	Not connected **Only applicable in SPD1179X/SPD1179Y**
30	HV Power	VPX_W	P	Pre-Driver W-Phase power FET switching node **Only applicable in SPD1179(Z)/SPD1176**
	-	NC	-	Not connected **Only applicable in SPD1179X/SPD1179Y**
31	HV IO	OUTH_W	O	Pre-Driver W-Phase high side FET gate drive **Only applicable in SPD1179(Z)/SPD1176**
	-	NC	-	Not connected **Only applicable in SPD1179X/SPD1179Y**
32	HV IO	OUTL_V	O	Pre-Driver V-Phase low side FET gate drive
33	HV Power	VPX_V	P	Pre-Driver V-Phase power FET switching node
34	HV IO	OUTH_V	O	Pre-Driver V-Phase high side FET gate drive
35	HV IO	OUTL_U	O	Pre-Driver U-Phase low side FET gate drive
36	HV Power	VPX_U	P	Pre-Driver U-Phase power FET switching node
37	HV IO	OUTH_U	O	Pre-Driver U-Phase high side FET gate drive
38	HV IO	MON	I	High voltage input for level monitor
39	HV IO	LIN	I/O	LIN bus interface, can be set as input or output.
40	HV Power	LIN_GND	P	LIN bus ground
41	5V I/O	XRSTn	I	Device reset pin, reset the device when low
42	3.3V Power	DVDD33	P	3.3 V digital power **Add 4.7uF and 0.1uF bypass ceramic cap to GND**
43	Ground	GND	G	Ground
44	-2V ~ 3.3V input	PGAIN	AI	Differential PGA negative input

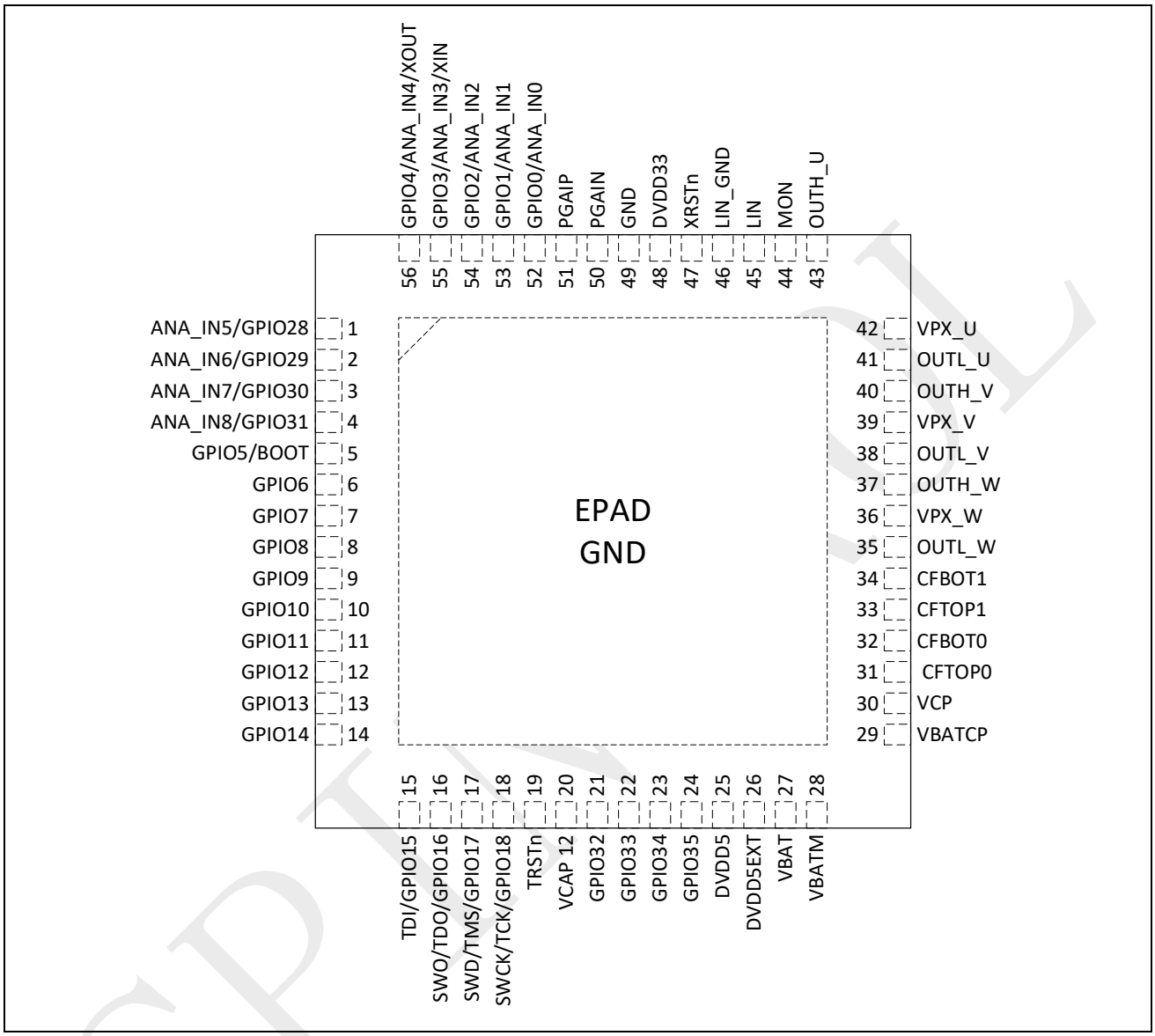
45	-2V ~ 3.3V input	PGAIP	AI	Differential PGA positive input
46	3.3V I/O	GPIO0	I/O	General-purpose input/output 0
		ANA_IN0	AI	Analog input channel 0
		PWMSOCAO	O	PWMSOCA output
		PWMSOCCO	O	PWMSOCC output
47	3.3V I/O	GPIO1	I/O	General-purpose input/output 1
		ANA_IN1	AI	Analog input channel 1
		PWMSOCB	O	PWMSOCB output
		ECAP_APWMO	O	APWM mode output of the ECAP
48	3.3V I/O	GPIO2	I/O	General-purpose input/output 2
		ANA_IN2	AI	Analog input channel 2
		DCLK	O	Clock output from CLKDET module for monitoring
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZ0O or EPWRTZ1O.
EPAD	Ground	GND	G	Exposed pad, connect to ground

[1] I = digital input, O = digital output or High-Voltage module output, AI = analog input, AO = analog output, P = power supply, G = ground.

[2] **All GPIO pins can be configured as ECAP input**.

3.2 QFN56

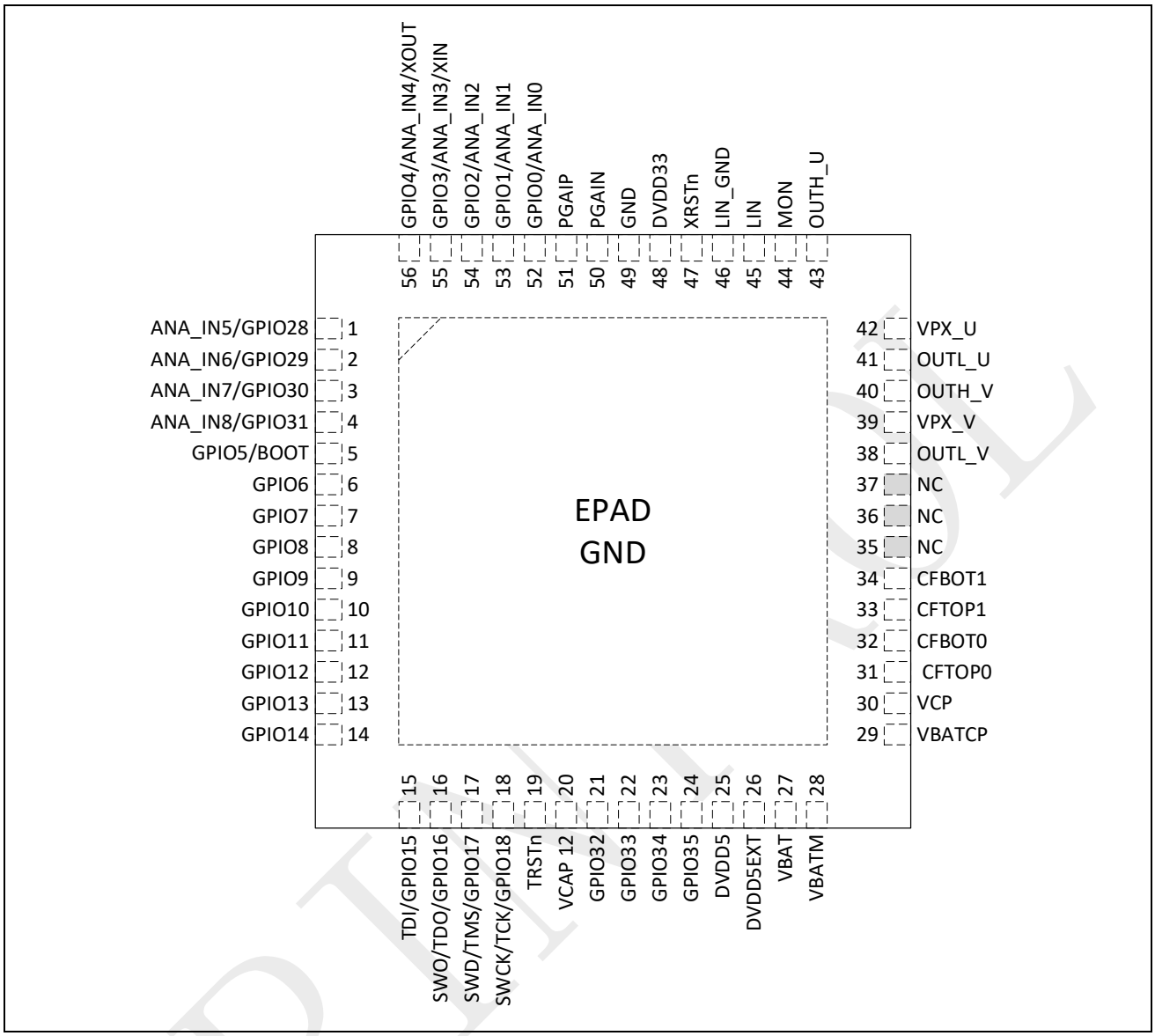
Figure 3-3: SPD1179 QFN56 pinout



[1] The figure above shows top view for the package.

[2] When TRSTn is high, GPIO15 ~ GPIO18 may be used for debug interface as shown in Table 2-1.

Figure 3-4: SPD1179X/SPD1179Y QFN56 pinout



[1] The figure above shows top view for the package.

[2] When TRSTn is high, GPIO15 ~ GPIO18 may be used for debug interface as shown in Table 2-1.

Table 3-2: SPD1179 QFN56 pin definitions

Pin	Type	Signal	Sub-Type[1]	Description
1	3.3V I/O	GPIO28	I/O	General-purpose input/output 28
		ANA_IN5	AI	Analog input channel 5
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWMSOCAO	O	PWMSOCA output
2	3.3V I/O	GPIO29	I/O	General-purpose input/output 29
		ANA_IN6	AI	Analog input channel 6
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWMSOCBO	O	PWMSOCB output
3	3.3V I/O	GPIO30	I/O	General-purpose input/output 30
		ANA_IN7	AI	Analog input channel 7
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWMSOCCO	O	PWMSOCC output
4	3.3V I/O	GPIO31	I/O	General-purpose input/output 31
		ANA_IN8	AI	Analog input channel 8
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWMSYNCO	O	PWMSYNC output
5	5V I/O	GPIO5 (BOOT)	I/O	General-purpose input/output 5 (BOOT)
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZ0O or EPWRTZ1O.
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		ECAP_APWMO	O	APWM mode output of the ECAP
6	5V I/O	GPIO6	I/O	General-purpose input/output 6
		SPI0_SCLK	I/O	SPI0 clock input/output
		UART1_TXD	O	UART1 transmitted data
		COMP_MON2	O	Comparator output monitor 2
7	5V I/O	GPIO7	I/O	General-purpose input/output 7
		SPI0_SFRM	I/O	SPI0 frame signal input/output
		UART1_RXD	I	UART1 received data
		COMP_MON3	O	Comparator output monitor 3
8	5V I/O	GPIO8	I/O	General-purpose input/output 8
		SPI0_MOSI	I/O	SPI0 master output, slave input
		CAN_TXD	O	SPI0 master input, slave output
		COMP_MON4	O	Comparator output monitor 4
9	5V I/O	GPIO9	I/O	General-purpose input/output 9
		SPI0_MISO	I/O	SPI0 master input, slave output
		CAN_RXD	I	SPI0 master output, slave input
		COMP_MON5	O	Comparator output monitor 5
10	5V I/O	GPIO10	I/O	General-purpose input/output 10
		UART0_TXD	O	UART0 transmitted data
		PWM0A	O	PWM0 output A
		I2C_SCL	I/O	I2C clock
11	5V I/O	GPIO11	I/O	General-purpose input/output 11

		UART0_RXD	I	UART0 received data
		PWM0B	O	PWM0 output B
		I2C_SDA	I/O	I2C data
12	5V I/O	GPIO12	I/O	General-purpose input/output 12
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWM1A	O	PWM1 output A
		PWM3A	O	PWM3 output A
13	5V I/O	GPIO13	I/O	General-purpose input/output 13
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWM1B	O	PWM1 output B
		PWM3B	O	PWM3 output B
14	5V I/O	GPIO14	I/O	General-purpose input/output 14
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWM2A	O	PWM2 output A
		I2C_SCL	I/O	I2C clock
15	5V I/O	GPIO15	I/O	General-purpose input/output 15
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWM2B	O	PWM2 output B
		I2C_SDA	I/O	I2C data
		TDI	I	JTAG data input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
16	5V I/O	GPIO16	I/O	General-purpose input/output 16
		UART1_TXD	O	UART1 transmitted data
		CAN_TXD	O	CAN transmitted data
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		TDO/SWO	O	JTAG data output or Asynchronous TRACE output
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
17	5V I/O	GPIO17	I/O	General-purpose input/output 17
		UART1_RXD	I	UART1 received data
		CAN_RXD	I	CAN received data
		SPI1_SCLK	I/O	SPI1 clock input/output
		TMS/SWD	I/O	JTAG mode select or SWD data
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
18	5V I/O	GPIO18	I/O	General-purpose input/output 18
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		PWMSYNCO	O	PWMSYNC output
		ECAP_APWMO	O	APWM mode output of the ECAP
		TCK/SWCK	I	JTAG clock or SWD clock
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
19	5V I/O	TRSTn	I	JTAG reset pin, reset the JTAG when low
20	1.2V Power	VCAP12	P	1.2 V power **Add 2.2uF and 0.1uF bypass ceramic cap to GND**
21	5V I/O	GPIO32	I/O	General-purpose input/output 32

		UART1_TXD	O	UART1 transmitted data
		I2C_SCL	I/O	I2C clock
		COMP_MON6	O	Comparator output monitor 6
22	5V I/O	GPIO33	I/O	General-purpose input/output 33
		UART1_RXD	I	UART1 received data
		I2C_SDA	I/O	I2C data
		COMP_MON7	O	Comparator output monitor 7
23	5V I/O	GPIO34	I/O	General-purpose input/output 34
		CAN_TXD	O	CAN transmitted data
		I2C_SCL	I/O	I2C clock
		EPWRTZ0O	O	EPWRTZ0 output for monitoring
24	5V I/O	GPIO35	I/O	General-purpose input/output 35
		CAN_RXD	I	CAN received data
		I2C_SDA	I/O	I2C data
		EPWRTZ1O	O	EPWRTZ1 output for monitoring
25	5V Power	DVDD5	P	5 V digital power **Add 2.2uF and 0.1uF bypass ceramic cap to GND**
26	5V Power	DVDD5EXT	P	5 V power for external loading **Add 2.2uF and 100nF bypass ceramic cap to GND**
27	HV Power	VBAT	P	High voltage power from 5.5V to 42V **Add 2.2uF and 0.1uF bypass ceramic cap to GND**
28	HV Power	VBATM	P	High voltage power for vds monitor from 5.5V to 42V **Add 0.1uF bypass ceramic cap to GND. Series 33 Ohm resistor from VBAT_D (VBAT for driver).**
29	HV Power	VBATCP	P	High voltage power for charge-pump from 5.5V to 42V **Add 2.2uF bypass ceramic cap to GND. Series 2 Ohm resistor from VBAT_D (VBAT for driver).**
30	HV Power	VCP	P	Charge-pump output voltage, maximum up to 48V. **Add 2.2uF ceramic cap to VBAT_D (VBAT for driver).**
31	HV Power	CFTOP0	P	Charge pump flying capacitor 0 top plate voltage **Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0**
32	HV Power	CFBOT0	P	Charge pump flying capacitor 0 bottom plate voltage **Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0**
33	HV Power	CFTOP1	P	Charge pump flying capacitor 1 top plate voltage

				Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1
34	HV Power	CFBOT1	P	Charge pump flying capacitor 1 bottom plate voltage **Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1**
35	HV IO	OUTL_W	O	Pre-Driver W-Phase low side FET gate drive **Only applicable in SPD1179**
	-	NC	-	Not connected **Only applicable in SPD1179X/SPD1179Y**
36	HV Power	VPX_W	P	Pre-Driver W-Phase power FET switching node **Only applicable in SPD1179**
	-	NC	-	Not connected **Only applicable in SPD1179X/SPD1179Y**
37	HV IO	OUTH_W	O	Pre-Driver W-Phase high side FET gate drive **Only applicable in SPD1179**
	-	NC	-	Not connected **Only applicable in SPD1179X/SPD1179Y**
38	HV IO	OUTL_V	O	Pre-Driver V-Phase low side FET gate drive
39	HV Power	VPX_V	P	Pre-Driver V-Phase power FET switching node
40	HV IO	OUTH_V	O	Pre-Driver V-Phase high side FET gate drive
41	HV IO	OUTL_U	O	Pre-Driver U-Phase low side FET gate drive
42	HV Power	VPX_U	P	Pre-Driver U-Phase power FET switching node
43	HV IO	OUTH_U	O	Pre-Driver U-Phase high side FET gate drive
44	HV IO	MON	I	High voltage input for level monitor
45	HV IO	LIN	I/O	LIN bus interface, can be set as input or output.
46	HV Power	LIN_GND	P	LIN bus ground
47	5V I/O	XRSTn	I	Device reset pin, reset the device when low
48	3.3V Power	DVDD33	P	3.3 V digital power **Add 4.7uF and 0.1uF bypass cap to GND**
49	Ground	GND	G	Ground
50	-2V ~ 3.3V input	PGAIN	AI	Differential PGA negative input
51	-2V ~ 3.3V input	PGAIP	AI	Differential PGA positive input
52	3.3V I/O	GPIO0	I/O	General-purpose input/output 0
		ANA_IN0	AI	Analog input channel 0
		PWMSOCAO	O	PWMSOCA output
		PWMSOCCO	O	PWMSOCC output
53	3.3V I/O	GPIO1	I/O	General-purpose input/output 1
		ANA_IN1	AI	Analog input channel 1
		PWMSOCB	O	PWMSOCB output
		ECAP_APWMO	O	APWM mode output of the ECAP

54	3.3V I/O	GPIO2	I/O	General-purpose input/output 2
		ANA_IN2	AI	Analog input channel 2
		DCLK	O	Clock output from CLKDET module for monitoring
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZ0O or EPWRTZ1O.
55	3.3V I/O	GPIO3	I/O	General-purpose input/output 3
		ANA_IN3	AI	Analog input channel 3
		XIN	AI	External oscillator input
		COMP_MON0	O	Comparator output monitor 0
56	3.3V I/O	GPIO4	I/O	General-purpose input/output 4
		ANA_IN4	AI	Analog input channel 4
		XOUT	O	External oscillator output
		COMP_MON1	O	Comparator output monitor 1
EPAD	Ground	GND	G	Exposed pad, connect to ground

[1] I = digital input, O = digital output or High-Voltage module output, AI = analog input, AO = analog output, P = power supply, G = ground.

[2] **All GPIO pins can be configured as ECAP input**.

3.3 GPIO pin function and state after reset

Table 3-3: GPIO pin function and state after reset

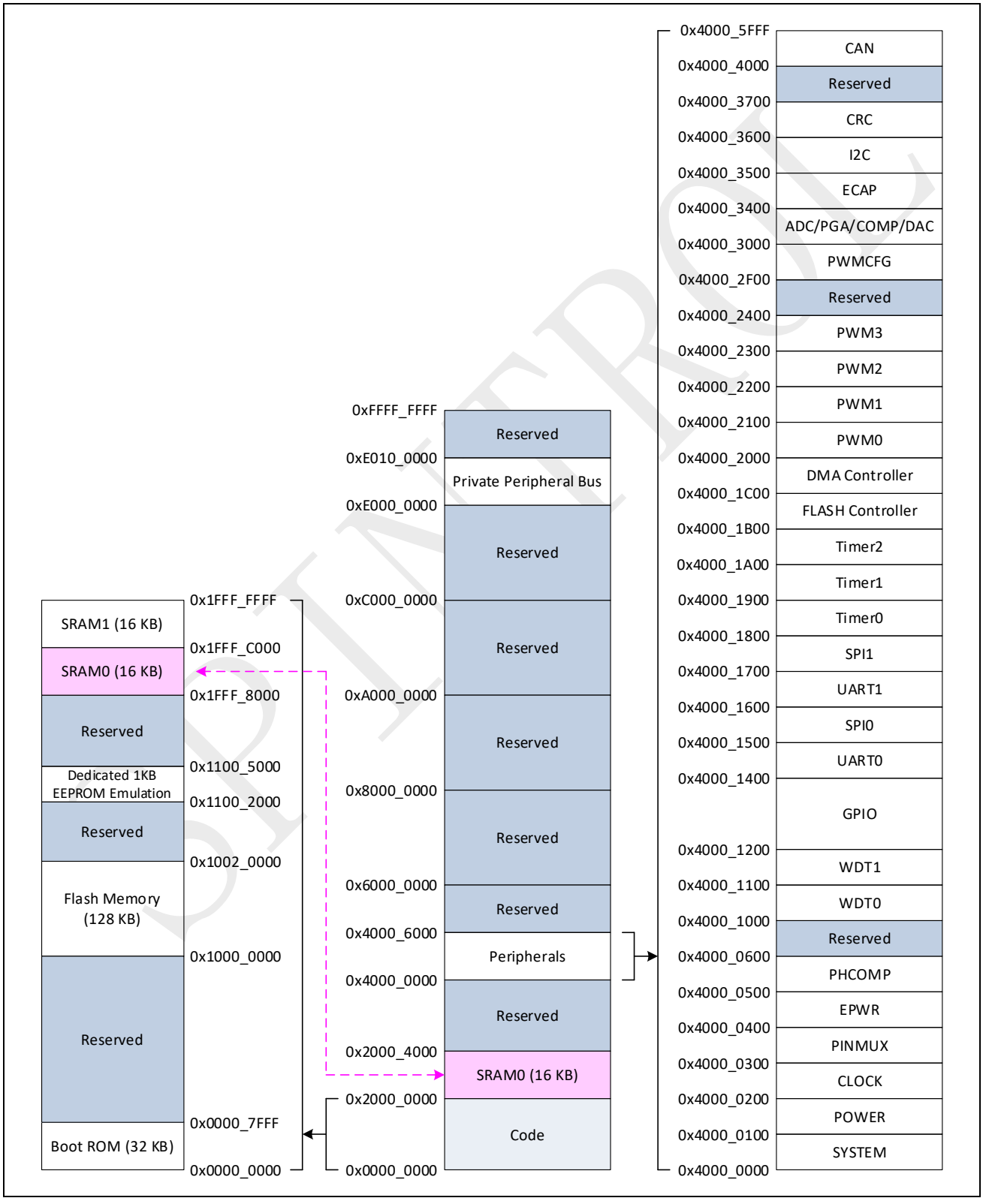
Pin Name	Default Function	Default State
GPIO0	ANA_IN0	Floating
GPIO1	ANA_IN1	Floating
GPIO2	ANA_IN2	Floating
GPIO3	ANA_IN3	Floating
GPIO4	ANA_IN4	Floating
GPIO5	GPIO5/BOOT	Pull down
GPIO6	GPIO6	Pull up
GPIO7	GPIO7	Pull up
GPIO8	GPIO8	Pull up
GPIO9	GPIO9	Pull up
GPIO10	GPIO10	Pull up
GPIO11	GPIO11	Pull up
GPIO12	GPIO12	Floating
GPIO13	GPIO13	Floating
GPIO14	GPIO14	Pull up
GPIO15	GPIO15	Pull up
GPIO16	GPIO16	Pull up
GPIO17	GPIO17	Pull up
GPIO18	GPIO18	Pull down
GPIO19	GPIO19	Floating
GPIO20	GPIO20	Floating
GPIO21	GPIO21	Floating
GPIO22	GPIO22	Floating
GPIO23	GPIO23	Floating
GPIO24	GPIO24	Floating
GPIO25	GPIO25	Pull up
GPIO26	GPIO26	Pull up
GPIO27	GPIO27	Pull down
GPIO28	ANA_IN5	Floating
GPIO29	ANA_IN6	Floating
GPIO30	ANA_IN7	Floating
GPIO31	ANA_IN8	Floating
GPIO32	GPIO32	Pull up
GPIO33	GPIO33	Pull up
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up

[1] In SPD1179/SPD1176, GPIO19 ~ GPIO27 are internally connected to the High Voltage module as shown in Figure 1-1, and not bonded out to the external pin. GPIO19 ~ GPIO24 are internally connected to the Pre-Driver module; GPIO25/GPIO26 are internally connected to LIN transceiver; GPIO27 is internally connected to the MON module.

4 Memory mapping

The memory map of SPD1179/SPD1176 is shown in Figure 4-1.

Figure 4-1: Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings[1][2]

Symbol	Parameter		Min	Max	Unit
V_{VBAT}[7]	Battery supply voltage for internal power system and LIN bus		-0.3	42	V
V_{VBATM}[7]	Monitor pin for external supply of power MOS		-0.3	42	V
V_{VBATCP}[7]	Battery supply voltage for internal charge-pump and pre-driver		-0.3	42	V
V_{LIN}	LIN bus interface, with respect to V_{LIN_GND}		-28	42	V
V_{MON}	High voltage input for level monitor		-28	42	V
V_{VCP}	Charge-pump voltage		-0.3	48	V
V_{VCP} - V_{VBATCP}	Charge-pump voltage minus battery supply voltage for internal charge-pump		-0.3	15.8	V
V_{VPX_X}[4]	Pre-driver floating ground		-10	42	V
V_{OUTH_X}[4]	Pre-driver high side output		-10	48	V
V_{OUTH_X} vs V_{PX_X}[4]	Pre-driver high side versus floating ground		-0.3	11[5]	V
V_{OUTL_X}[4]	Pre-driver low side output		-0.3	11[5]	V
V_{DVDD5}	DVDD5 voltage range for internal block		-0.3	6.5	V
$V_{DVDD5EXT}$	VDD5EXT voltage range for external circuit		-0.3	6.5	V
V_{DVDD33}	DVDD33 voltage range for internal MCU		-0.3	4.6	V
V_{VCAP12}	VCAP12 voltage range for internal MCU core		-0.3	1.5	V
V_{IN_5V}	5V IO input voltage		-0.3	V_{DVDD5}+0.3	V
V_{IN_3V}	3.3V IO input voltage		-0.3	V_{DVDD33}+0.3	V
V_{LIN_GND}[6]	LIN bus ground.		-0.3	0.3	V
I_{IC}	Input clamp current		-20	+20	mA
I_{OC}	Output clamp current		-20	+20	mA
T_J	Junction temperature[3]	SPD1179	-40	+150	°C
		SPD1176	-40	+125	°C
$t_{T,J,150}$	Time that the SPD1179 can run continuously at T_J=150°C		2000	-	h
T_{stg}	Storage temperature[3]		-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.
[2] All voltage values are with respect to V_{GND}, unless otherwise noted.
[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.
[4] X=U or V or W.
[5] Limited by design, internal circuit will turn on to clamp this voltage level.
[6] Short LIN_GND and GND on PCB board.
[7] Power ramp-up speed must be less than 0.1V/us, otherwise the device may be damaged permanently.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{VBAT}	Battery supply voltage for internal power system and LIN bus	-	5.5	-	28	V
	Extend range[1] for V_{VBAT}		28		40	V
V_{VBATM}	Battery supply voltage for internal pre-driver	-	5.5	-	28	V
	Extend range[1] for V_{VBATM}		28		40	V
V_{VBATCP}	Battery supply voltage for internal charge-pump	-	5.5	-	28	V
	Extend range[1] for V_{VBATCP}		28		40	V
V_{DVDD5}	DVDD5 voltage range for internal block	-	4.5	5.0	5.5	V
$V_{DVDD5EXT}$	VDD5EXT voltage range for external loading	-	4.5	5.0	5.5	V
V_{DVDD33}	DVDD33 voltage range for internal MCU	-	2.97	3.3	3.63	V
V_{VCAP12}	VCAP12 voltage range for internal MCU core	-	1.08	1.2	1.32	V
V_{GND}	Supply ground	-	-	0	-	V
V_{IH_5V}	5V high-level input voltage	V_{DVDD5} = 5 V	-	3.5	V_{DVDD5}+0.3	V
V_{IL_5V}	5V low-level input voltage	V_{DVDD5} = 5 V	V_{GND}-0.3	1.5	-	V
I_{OH_5V}	5V high-level output source current when V_{OH} = 4.0V, V_{DVDD5}=4.5V	STRENGTH=0 STRENGTH=1	-	-	0.4 7.3	mA
I_{OL_5V}	5V low-level output sink current when V_{OL} = 0.4V, V_{DVDD5}=4.5V	STRENGTH=0 STRENGTH=1	-	-	1.74 26.1	mA
V_{IH_3V}	3.3V high-level input voltage	V_{DVDD33} = 3.3 V	2.0	-	V_{DVDD33}+0.3	V
V_{IL_3V}	3.3V low-level input voltage	V_{DVDD33} = 3.3 V	V_{GND}-0.3	-	0.8	V
I_{OH_3V}	3.3V high-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL_3V}	3.3V low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
T_J	Junction temperature	SPD1179	-40	-	+150	°C
		SPD1176	-40	-	+125	°C

[1] This extend voltage range is only allowed for a short duration: tmax≤400 ms and with parameter deviation for function. Continuous operation at this extend voltage range is not allowed. This feature is not specifically stated in the subsequent tables, and it has this meaning.

5.3 I/O Electrical characteristics

Table 5-3: 5V IO Electrical characteristics (V_{DVDD5} = 5V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	V_{DVDD5}-0.5	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	-	-	0.5	V
V_{IH}	High-level input voltage	-	3.5	-	V_{DVDD5}+0.3	V
V_{IL}	Low-level input voltage	-	V_{GND}-0.3	-	1.5	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1	-	-	0.4 7.3	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1	-	-	1.74 26.1	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down both disabled)	V_{IH} = 0 V	-	-	10	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down both disabled)	V_{IH} = V_{DVDD5}	-	-	10	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	-	50	-	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DVDD5}	-	50	-	kΩ

Table 5-4: 3.3V IO Electrical characteristics (V_{DVDD33} = 3.3V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	V_{DVDD33}-0.4	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	-	-	0.4	V
V_{IH}	High-level input voltage	-	2.0	-	V_{DVDD33}+0.3	V
V_{IL}	Low-level input voltage	-	V_{GND}-0.3	-	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down both disabled)	V_{DVDD33} = 3.3V, V_{IH} = 0 V	-	-	10	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down both disabled)	V_{DVDD33} = 3.3V, V_{IH} = V_{DVDD33}	-	-	10	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	-	41	-	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DVDD33}	-	42	-	kΩ

5.4 Power mode transition time

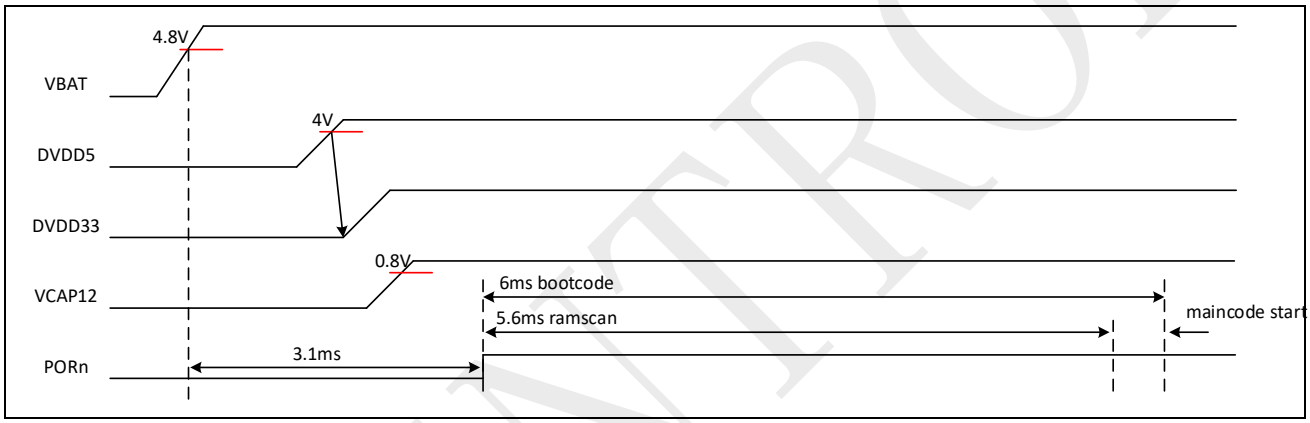
Table 5-5: Power mode transition time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{stop,entry}$	Stop mode entry time	-	-	25	-	us
$t_{stop,exit}$	Stop mode exit time (to user's code)	-	-	1	-	ms
$t_{sleep,entry}$	Sleep mode entry time	-	-	25	-	us
$t_{sleep,exit}$[1]	Sleep mode exit time (to user's code)	-	-	7.4	-	ms
$t_{power-up}$[2]	Cold power-up time (to user's code)	-	-	9.1	-	ms

[1] It contain ~5.63ms for the RAM self-test.

[2] Compared with sleep mode exit time, it contain extra ~1.7ms POR time for VBAT.

Figure 5-1: Cold power-up transition time



5.5 Power consumption

Typical current consumption

In active mode, the SPD1179/SPD1176 is placed under the following conditions:
- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are enabled;
- All peripheral clocks are as fast as HCLK (frequency division is 1), except DGCLK (Max 50 MHz);
- All clock modules are enabled;
- Select PLL clock as system clock source.
- Charge pump enable, Pre-driver toggle and no external driver MOS.
- GPIO5 is connected to GND

In stop mode, the SPD1179/SPD1176 is placed under the following conditions:
- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO, ROSC and XO) are disabled;
- 5V/3.3V/1.2V LDOs are in low power mode;
- GPIO5 is connected to GND

In sleep mode, the SPD1179/SPD1176 is placed under the following conditions:
- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are disabled;

- Clock modules (PLL, RCO, ROSC and XO) are disabled;
- 5V/3.3V/1.2V LDOs are shut down to 0V;
- GPIO5 is connected to GND

The typical operational current consumption over various HCLK frequency is shown in Figure 5-2.

Figure 5-2: Typical operational current versus frequency

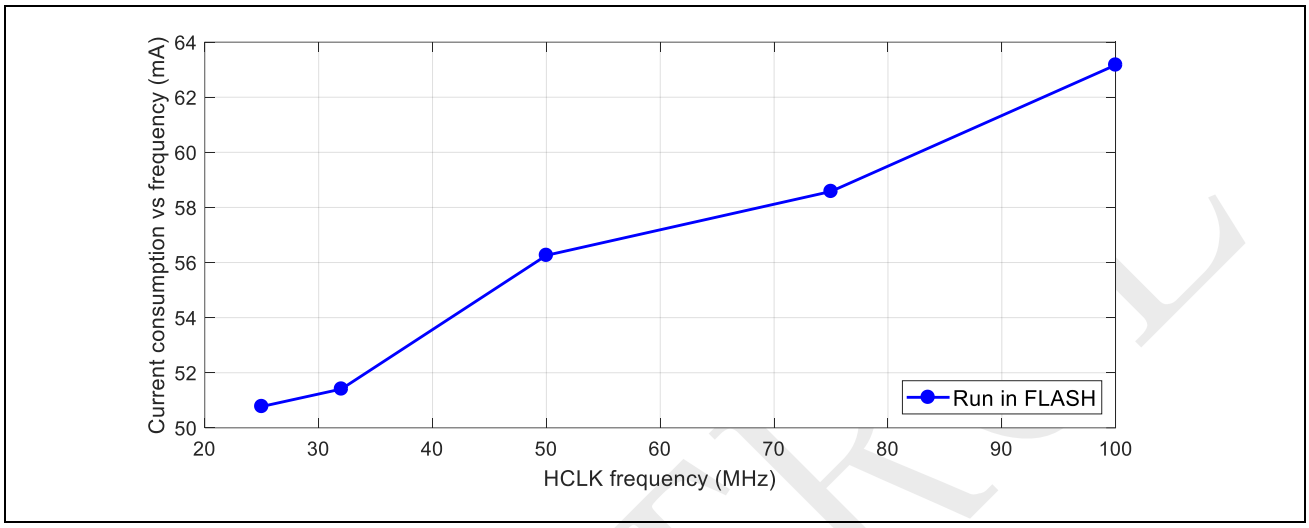


Table 5-6: SPD1179/SPD1176 current consumption (V_{VBAT} = 18V)

Conditions	Junction Temperature T_J (°C)						Unit
	25	85	105	125	150	175	
Active mode (f_{HCLK} = f_{PLL} = 100 MHz)	68.000	66.600	67.100	68.700	71.200	75.500	mA
Active mode (f_{HCLK} = f_{PLL} = 32 MHz)	51.300	51.800	52.500	53.900	56.800	61.200	mA
Stop mode[1]	0.180	1.070	1.830	-	-	-	mA
Sleep mode	0.038	0.046	0.049	0.058	0.095	0.264	mA

[1] Stop mode support T_J from -40°C to 105°C.

Table 5-7: SPD1179/SPD1176 active current consumption (V_{VBAT} = 28V)

Conditions	Junction Temperature T_J (°C)						Unit
	25	85	105	125	150	175	
Active mode (f_{HCLK} = f_{PLL} = 100 MHz)	68.620	66.900	67.300	68.500	71.100	75.200	mA
Active mode (f_{HCLK} = f_{PLL} = 32 MHz)	51.900	52.400	52.700	53.700	56.470	61.100	mA
Stop mode[1]	0.190	1.080	1.840	-	-	-	mA
Sleep mode	0.045	0.056	0.063	0.073	0.117	0.279	mA

[1] Stop mode support T_J from -40°C to 105°C.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 5-8. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
  - With all peripherals clocked disabled
  - With only one peripheral enabled

Table 5-8: Peripheral current consumption

Peripherals[1]	Conditions	Typ[2]	Unit
BOD	Select RCO as system clock source; All other peripherals are in default settings	106.0	uA
ADC[3]	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK; f_{HCLK} = 100 MHz, f_{PLL} = 100 MHz	8854.0	uA
Monitoring ADC[3]		2989.0	uA
T-Sensor		157.0	uA
DPGA[4]		1106.0	uA
SPGA[4]		156.0	uA
DAC buffer		274.0	uA
DAC		327.0	uA
Phase Comparator		126.0	uA
Comparator		105.0	uA
UART	UART clock 100MHz, 512000 bps	383.0	uA
SPI	SPI clock 100MHz, 20Mbps	284.0	uA
I2C	I2C clock 100MHz, 100Kbps	436.0	uA
CAN	CAN clock 100MHz, 1Mbps + 8Mbps	3526.0	uA
PWM (Without Pre-Driver)	PWM clock 100MHz and toggle frequency 15kHz	302.5	uA
PWM (With Pre-Driver)	PWM clock 100MHz, PWM toggle frequency 15kHz	6064.0	uA
ECAP	ECAP clock 100MHz	324.0	uA
WDT	WDT clock 100MHz	220.0	uA
TIMER	TIMER clock 100MHz	144.0	uA
FLASH	HCLK clock 100MHz	306.0	uA
XO	HCLK is from 100MHz PLL, which takes RCO as input	736.0	uA
RCO	HCLK is from 100MHz PLL, which takes XO (32MHz) as input	254.0	uA
PLL	XO (32MHz) as HCLK source, f_{PLL} = 100 MHz	961.0	uA
LIN transceiver	UART clock 100MHz, 19200bps	480.0	uA
DVDD5EXT	-	42.4	uA

[1] For peripherals with multiple instances, the current quoted is for single modules (result of average).
[2] Typical values are measured at T_A = 25 °C, V_{VBAT} = 12 V.
[3] ADC analog current contain ADC analog module, bandgap and ADC reference buffer.
[4] The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

5.6 BOD characteristics

Table 5-9: VCAP12 BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(VCAP12OV)}$	VCAP12 over-voltage assert threshold	-	-	1.33	-	V
$V_{th0(VCAP12OV)}$	VCAP12 over-voltage release threshold	-	-	1.31	-	V
$V_{th1(VCAP12UV)}$	VCAP12 under-voltage assert threshold	-	-	1.1	-	V
$V_{th0(VCAP12UV)}$	VCAP12 under-voltage release threshold	-	-	1.14	-	V

Table 5-10: DVDD33 BOD0[1] characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(DVDD33OV)}$	DVDD33 over-voltage assert threshold	-	-	4.24	-	V
$V_{th0(DVDD33OV)}$	DVDD33 over-voltage release threshold	-	-	4.08	-	V
$V_{th1(DVDD33UV)}$	DVDD33 under-voltage assert threshold	-	-	2.58	-	V
$V_{th0(DVDD33UV)}$	DVDD33 under-voltage release threshold	-	-	2.65	-	V

[1] Brown-out detector for DVDD33 in MCU.

Table 5-11: DVDD33 BOD1[1] characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(DVDD33OV)}$	DVDD33 over-voltage assert threshold	-	-	4.22	-	V
$V_{th0(DVDD33OV)}$	DVDD33 over-voltage release threshold	-	-	4.06	-	V
$V_{th1(DVDD33UV)}$	DVDD33 under-voltage assert threshold	-	-	2.64	-	V
$V_{th0(DVDD33UV)}$	DVDD33 under-voltage release threshold	-	-	2.70	-	V

[1] Brown-out detector for DVDD33 in high voltage.

Table 5-12: VBAT BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(VBATOV)}$	VBAT over-voltage assert threshold	-	-	44.7	-	V
$V_{th0(VBATOV)}$	VBAT over-voltage release threshold	-	-	38.9	-	V
$V_{th1(VBATUV)}$	VBAT under-voltage assert threshold	-	-	4.95	-	V
$V_{th0(VBATUV)}$	VBAT under-voltage release threshold	-	-	5.13	-	V

Table 5-13: DVDD5 BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(DVDD5OV)}$	DVDD5 over-voltage assert threshold	-	-	5.92	-	V
$V_{th0(DVDD5OV)}$	DVDD5 over-voltage release threshold	-	-	5.84	-	V
$V_{th1(DVDD5UV)}$	DVDD5 under-voltage assert threshold	-	-	4.41	-	V
$V_{th0(DVDD5UV)}$	DVDD5 under-voltage release threshold	-	-	4.50	-	V

Table 5-14: DVDD5EXT BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(DVDD5EXTOV)}$	DVDD5EXT over-voltage assert threshold	-	-	5.89	-	V
$V_{th0(DVDD5EXTOV)}$	DVDD5EXT over-voltage release threshold	-	-	5.81	-	V
$V_{th1(DVDD5EXTUV)}$	DVDD5EXT under-voltage assert threshold	-	-	3.77	-	V
$V_{th0(DVDD5EXTUV)}$	DVDD5EXT under-voltage release threshold	-	-	3.91	-	V

Table 5-15: (VCP – VBAT) BOD characteristics

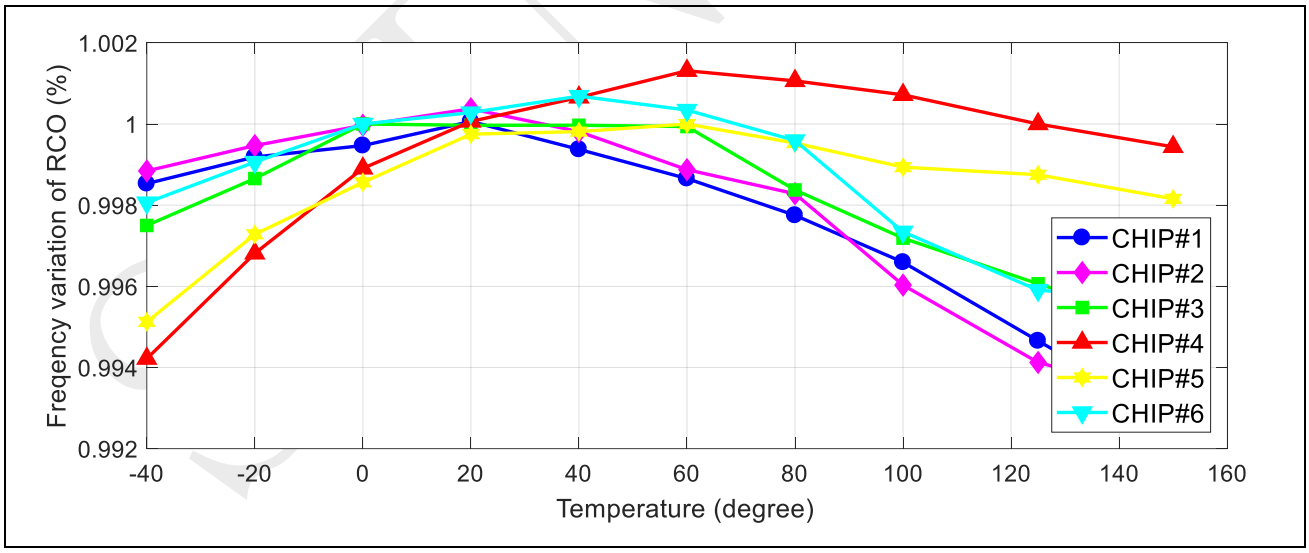
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1((VCP-VBAT)OV)}$	(VCP – VBAT) over-voltage assert threshold	-	-	14.81	-	V
$V_{th0((VCP-VBAT)OV)}$	(VCP –VBAT) over-voltage release threshold	-	-	14.57	-	V
$V_{th1((VCP-VBAT)UV)}$	(VCP –VBAT) under-voltage assert threshold	-	-	6.097	-	V
$V_{th0((VCP-VBAT)UV)}$	(VCP –VBAT) under-voltage release threshold	-	-	6.206	-	V

5.7 RCO characteristics

Table 5-16: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RCO}	RCO frequency at room temperature	T_J = 25 °C	31.936	32.00	32.064	MHz
E_{RCO}	RCO frequency error (RCO frequency variation versus temperature)	T_J = -40~150 °C	-1.5	-	1.5	%
t_{settle}	RCO frequency ready time	E_{RCO} < 1%	-	4.2	-	us

Figure 5-3: RCO frequency with temperature



5.8 PLL characteristics

Table 5-17: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{VCO}	VCO frequency	T_J = -40~150 °C	400	500	600	MHz
f_{PFD}[1]	Phase-Frequency Detector (PFD) input frequency	-	4	-	8	MHz
t_{lock}[1]	Locking time	T_J = 25 °C	-	10	15	us
t_{jitter}	PLL output clock jitter	T_J = 25 °C	-	40	-	ps

[1] Not subject to production test, guaranteed by design.

5.9 XO characteristics

Table 5-18: XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XO}	XO frequency	T_J = -40~150 °C	4	-	32	MHz

5.10 13-bit ADC characteristics

Table 5-19: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_R	Resolution	No missing code. Monotonic	13	-	-	bits
f_S	Conversion speed[1]	-	-	-	2.5	MSPS
V_{in}	Input voltage range	-	0	-	V_{DDA}	V
V_{ref}	Reference voltage	-	1.194	1.2	1.206	V
I_{on}	Operational current	V_{DVDD33} = 3.3 V	-	8.5	11.5	mA
INL	Integral linearity error	-	-3.0	-	3.0	LSB
DNL	Differential linearity	-	-1.0	-	1.5	LSB
E_{offset}	Offset error[2]	With calibration	-4	±2	4	LSB
E_{gain}	Gain error[2]	With calibration	-40	±4	40	LSB
T_{coef}	ADC temperature coefficient with internal reference	-	-	30	-	ppm/°C
t_{settle}[3]	Power-up time	-	-	-	100	us
$ENOB_{DC}$	DC Noise Floor	-	-	11.5	-	bits
SNR	Signal-to-noise ratio	f_{in} = 100kHz, V_{in} = 0.94FS, N = 8192	-	71	-	dBFS
THD	Total harmonic distortion		-	-84	-	dBFS
ENOB	Effective number of bits		-	11.4	-	bits
SFDR	Spurious free dynamic range		-	80	-	dBFS

[1] Sampling time = 200ns, conversion time = 200ns
[2] Offset and gain can be calibrated automatically by hardware.
[3] Not subject to production test, guaranteed by design.

5.11 Monitoring ADC characteristics

Table 5-20: Monitoring ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_R	Resolution	No missing code. Monotonic	13	-	-	bits
f_S	Conversion speed[1]	-	-	-	500	KSPS
V_{in}	Input voltage range	-	0	-	V_{DVDD33}	V
V_{ref}	Reference voltage	-	1.19	1.2	1.21	V
I_{on}	Operational current	V_{DVDD33} = 3.3 V	-	2.8	3.6	mA
INL	Integral linearity error	-	-3.0	-	3.0	LSB
DNL	Differential linearity	-	-1.0	-	1.0	LSB
E_{offset}	Offset error	With calibration	-4	±2	4	LSB
E_{gain}	Gain error	With calibration	-40	±4	40	LSB
$ENOB_{DC}$	DC Noise Floor	-	-	11.5	-	bits
SNR	Signal-to-noise ratio	f_{in} = 50kHz, V_{in} = 0.94FS, N = 4096	-	71	-	dBFS
THD	Total harmonic distortion		-	-84	-	dBFS
ENOB	Effective number of bits		-	11.4	-	bits
SFDR	Spurious free dynamic range		-	80	-	dBFS

[1] Sampling time = 1µs, conversion time = 1µs.

5.12 Temperature sensor characteristics

Table 5-21: Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$TMCU_{slope}$	When the temperature sensor is measured by the ADC, for each increase of 1 LSB in the ADC output code, the corresponding temperature value changes.	-	-	3.7	-	°C/LSB
$TPMU_{slope}$		-	-	-0.48	-	°C/LSB
$TLIN_{slope}$		-	-	-0.48	-	°C/LSB
$TMCU_{offset}$	The code obtained by ADC measuring the temperature sensor.	T_J = 25 °C	-	-81	-	LSB
$TPMU_{offset}$			-	-772.8	-	LSB
$TLIN_{offset}$			-	-772.8	-	LSB

5.13 DPGA characteristics

Table 5-22: DPGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Differential input range		-2.7/G	-	+2.7/G	V
V_{out}	Output voltage range	-	0.3	-	V_{DVDD33}-0.3	V
R_{in}	Input impedance	-	-	4	-	kΩ
G	Gain	Differential	2, 4, 8, 16, 24, 32, 48, 64			-
E_{gain}	Gain error	Differential Gain = 2	-1.5	-	1.5	%
		Differential Gain = 16	-1	-	1	%
		Differential Gain = 64	-1	-	1	%
V_{offset}	Offset	Differential Gain=2	-3	-	9	mV
		Differential Gain=16	-2		4	mV
		Differential Gain=64	-2		4	mV
V_{CM}	Common mode input voltage range	Differential gain = 2	-1.5	-	2	V
		Differential gain = 4	-0.9	-	2	V
		Differential gain = 8	-0.75	-	2	V
		Differential gain = 16	-0.6	-	2	V
		Differential gain = 24	-0.57	-	2	V
		Differential gain = 32	-0.55	-	2	V
		Differential gain = 48	-0.52	-	2	V
		Differential gain = 64	-0.5	-	2	V
t_{settle}	Settle time[1]	Differential gain = 2	-	313.7	441.6	ns
		Differential gain = 4	-	303.1	425.5	ns
		Differential gain = 8	-	268.4	423.8	ns
		Differential gain = 16	-	376.7	604.7	ns
		Differential gain = 24	-	355.8	598.9	ns
		Differential gain = 32	-	442.9	742.3	ns
		Differential gain = 48	-	628.0	1061.0	ns
		Differential gain = 64	-	813.3	1378.0	ns
GBW	Gain bandwitdth[2]	Differential gain = 2	6	9.68	-	MHz
		Differential gain = 4	3.8	6.07	-	MHz
		Differential gain = 8	2.56	3.45	-	MHz
		Differential gain = 16	1.37	1.85	-	MHz
		Differential gain = 24	1.23	1.63	-	MHz
		Differential gain = 32	0.93	1.23	-	MHz
		Differential gain = 48	0.63	0.83	-	MHz
		Differential gain = 64	0.4	0.63	-	MHz
SR	Slew rate[3]	Differential gain = 2	15	21	30	V/us
		Differential gain = 4	15	21	30	V/us
		Differential gain = 8	14.5	21	30	V/us
		Differential gain = 16	11.2	18.9	29.7	V/us
		Differential gain = 24	12.57	21	33.4	V/us
		Differential gain = 32	9.25	18.4	31.8	V/us
		Differential gain = 48	6.1	11.5	25	V/us

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Differential gain = 64	4.6	8.6	17.6	V/us
$ENOB_{DC}$	Effective number of bits	Differential Gain = 2	-	11.93	-	bits
		Differential Gain = 16	-	11.57	-	bits
		Differential Gain = 64	-	10.94	-	bits
SNR	Signal-to-noise ratio at 10kHz input	Differential Gain = 2	-	72.2	-	dBFS
		Differential Gain = 16	-	71.1	-	dBFS
		Differential Gain = 64	-	64.8	-	dBFS
THD	Total harmonic distortion at 10kHz input	Differential Gain = 2	-	79.59	-	dBFS
		Differential Gain = 16	-	81.29	-	dBFS
		Differential Gain = 64	-	78.47	-	dBFS
$CMRR_{DC}$	DC common mode rejection Ratio	Differential Gain = 2	-	-59.7	-	dBFS
		Differential Gain = 16		-52.6	-	dBFS
		Differential Gain = 64	-	-61	-	dBFS
$PSRR_{DC}$	Power Supply Rejection Ratio	Differential Gain = 2	-	-72.8	-	dBFS
		Differential Gain = 16	-	-84.9	-	dBFS
		Differential Gain = 64	-	-93.4	-	dBFS
I_{on}	Current consumption	Differential Gain=2	-	1.215	-	mA
		Differential Gain=16	-	1.096	-	mA
		Differential Gain=64	-	1.152	-	mA

[1] Settle time is measured by step input, and differential output change from -2.7V to 2.7V (V_{DVDD33}=3.3V), the time for output to be settled to 98%, guarantee by design.

[2] GBW data is guaranteed by design.

[3] Slew rate data is from 10% to 90% of output signal, guaranteed by design.

Figure 5-4: Settling time with different gain

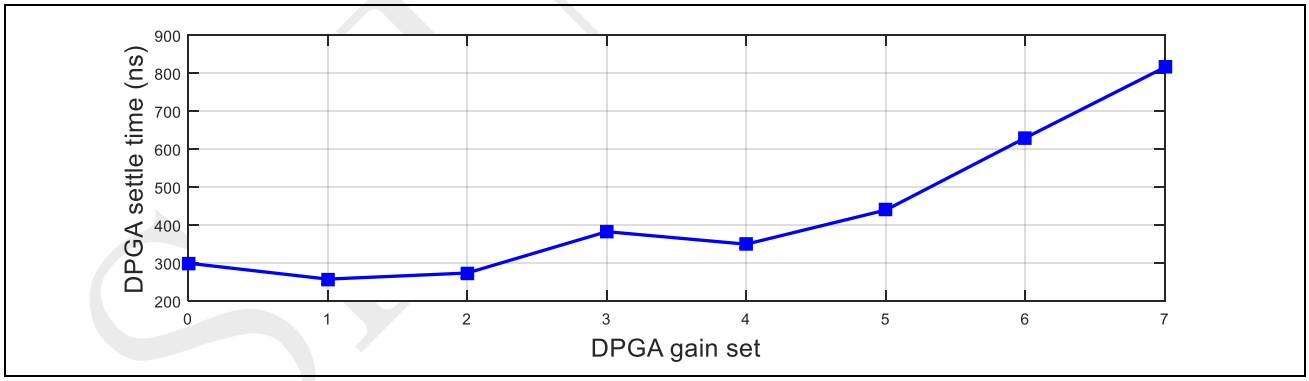


Figure 5-5: ENOB_DC with different gain

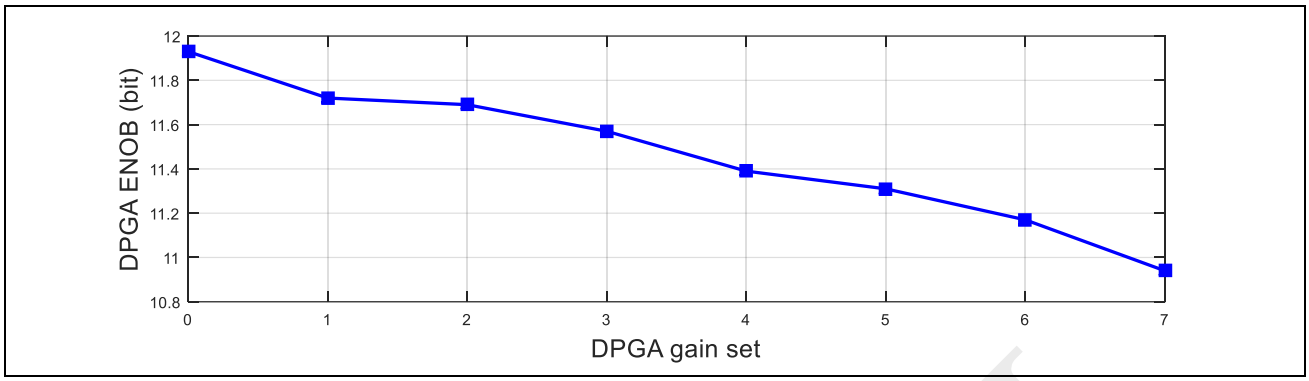


Figure 5-6: SNR with different gain

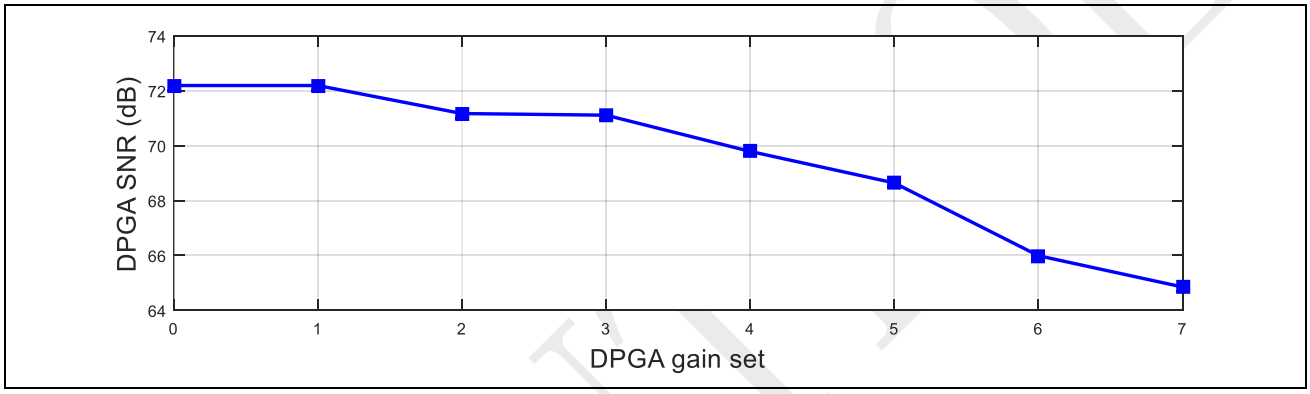


Figure 5-7: THD with different gain

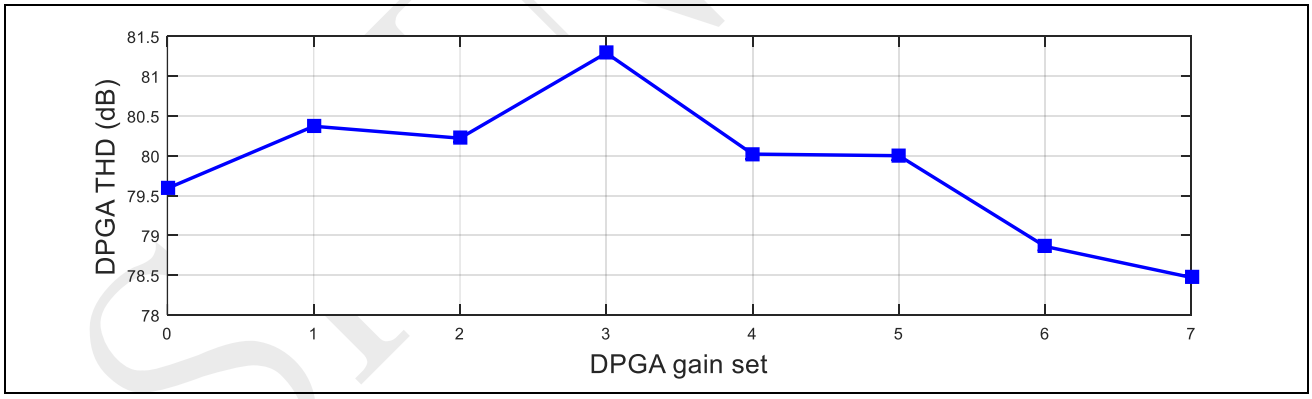


Figure 5-8: CMRR_DC with different gain

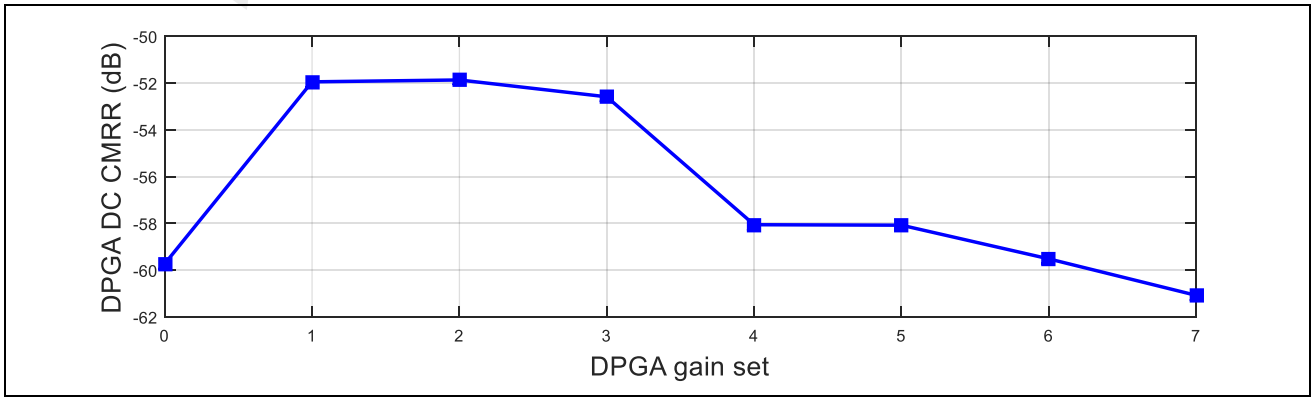
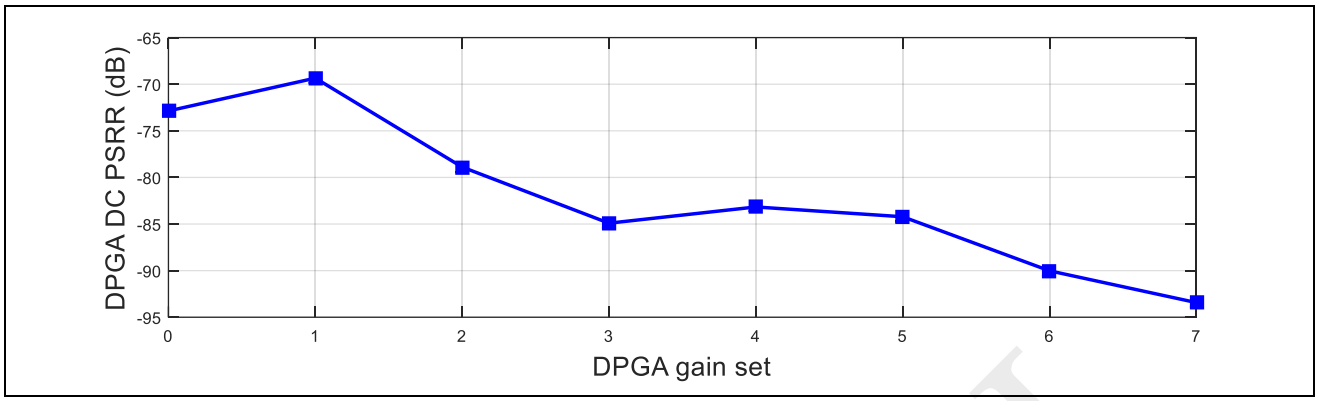


Figure 5-9: PSRR_DC with different gain



5.14 SPGA characteristics

Table 5-23: SPGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input range	-	0.3	-	V_{DDA}-1.3	V
V_{out}	Output voltage range	-	0.3	-	V_{DDA}-0.3	V
R_{in}	Input impedance	-	-	High-Z	-	Ω
G	Gain	Single-ended	1, 2, 4, 8, 16, 32, 48, 64			-
E_{gain}	Gain error	Gain = 2	-1	-	1	%
		Gain = 32	-1.2	-	1.2	%
		Gain = 64	-2	-	2	%
V_{offset}	Offset	-	-10	-	5	mV
t_{settle}	Settle time	Gain = 2	-	300	-	ns
		Gain = 32		1000	-	ns
		Gain = 64	-	2000	-	ns
ENOB	Effective number of bits	Gain = 2	-	11	-	bits
		Gain = 32	-	9	-	bits
		Gain = 64	-	8	-	bits
I_{on}	Current consumption	-	-	0.5	-	mA

Figure 5-10: Settling time with different gain

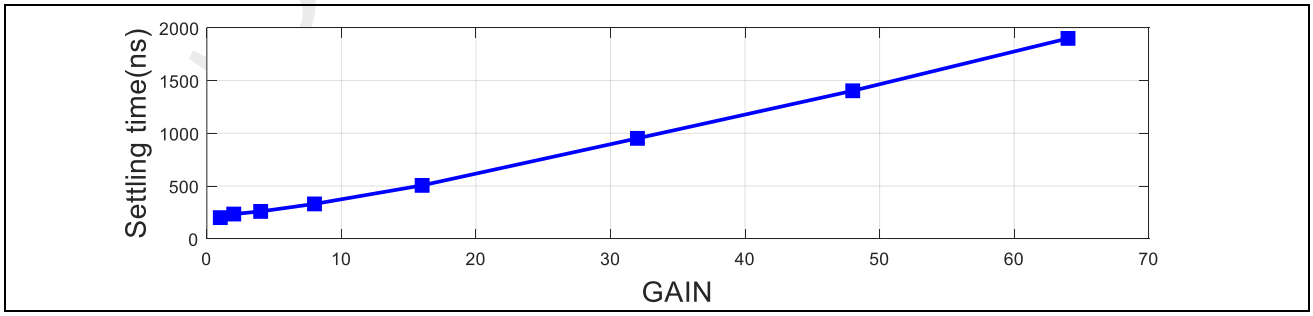
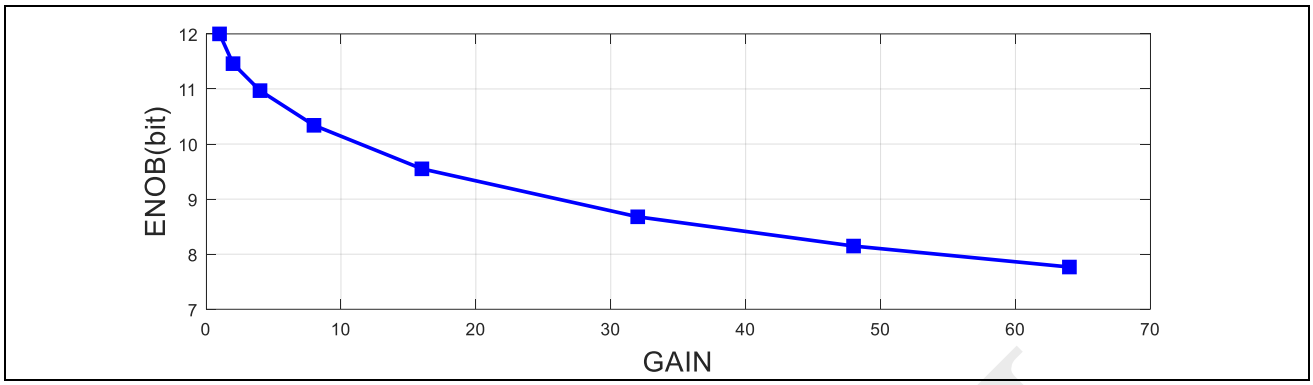


Figure 5-11: ENOB_DC with different gain



5.15 Analog comparator characteristics

Table 5-24: Analog comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage range	-	0	-	V_{DVDD33}	V
V_{offset}	Offset voltage (Hysteresis voltage option = 0)	V_{DVDD33} = 3.3V, T_J = 25°C, V_{cm} = 1.65V	-10	-	10	mV
V_{hyst}	Hysteresis voltage option = 0			0		mV
	Hysteresis voltage option = 1		-	13	-	mV
	Hysteresis voltage option = 2		-	25	-	mV
	Hysteresis voltage option = 3		-	37	-	mV
t_d	Delay time – comparator response time to PWM shunt down (Asynchronous)		-	50	-	ns

5.16 Phase comparator characteristics

Table 5-25: Phase comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage range	-	0	-	V_{DVDD33}	V
V_{offset}	Offset voltage (Hysteresis voltage=0)	V_{DVDD33} = 3.3V, T_J = 25°C, V_{cm} = 1.65V	-3.5	-	3.5	mV
V_{hyst}	Hysteresis voltage option = 0			0		mV
	Hysteresis voltage option = 1		-	13	-	mV
	Hysteresis voltage option = 2		-	25	-	mV
	Hysteresis voltage option = 3		-	37	-	mV
t_d	Delay time – comparator response time to PWM shunt down (Asynchronous)		-	250	-	ns

5.17 Internal 10-bit DAC characteristics

Table 5-26: DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N	Resolution	Monotonic	10	-	-	bit
V_{FS}	Full scale value	-	0	-	V_{DVDD33}	V
DNL	Differential linearity	-	-0.5	-	0.5	LSB
INL	Integral linearity	-	-1	-	1	LSB
E_{offset}	Offset error	-	-	5	-	mV
t_{settle}[1]	DAC settling time	-	-	-	1	us

[1] Guaranteed by design.

Figure 5-12: DNL curve

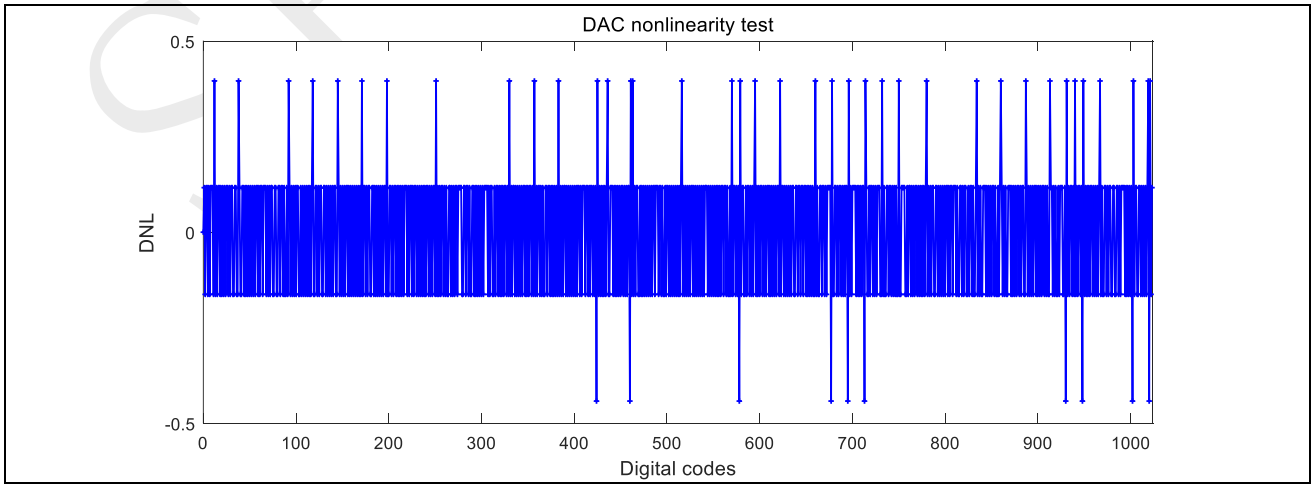
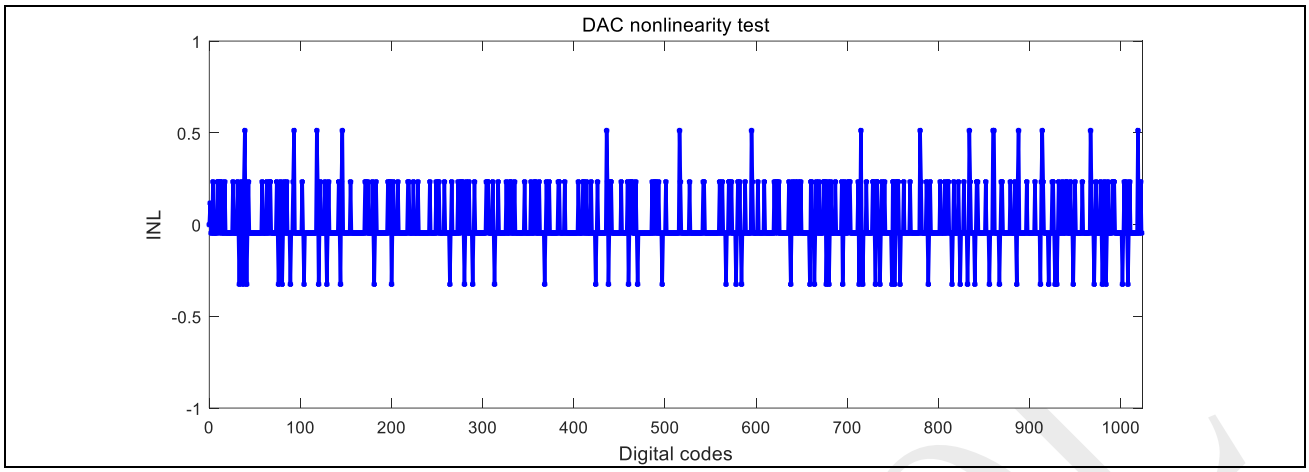


Figure 5-13: INL curve



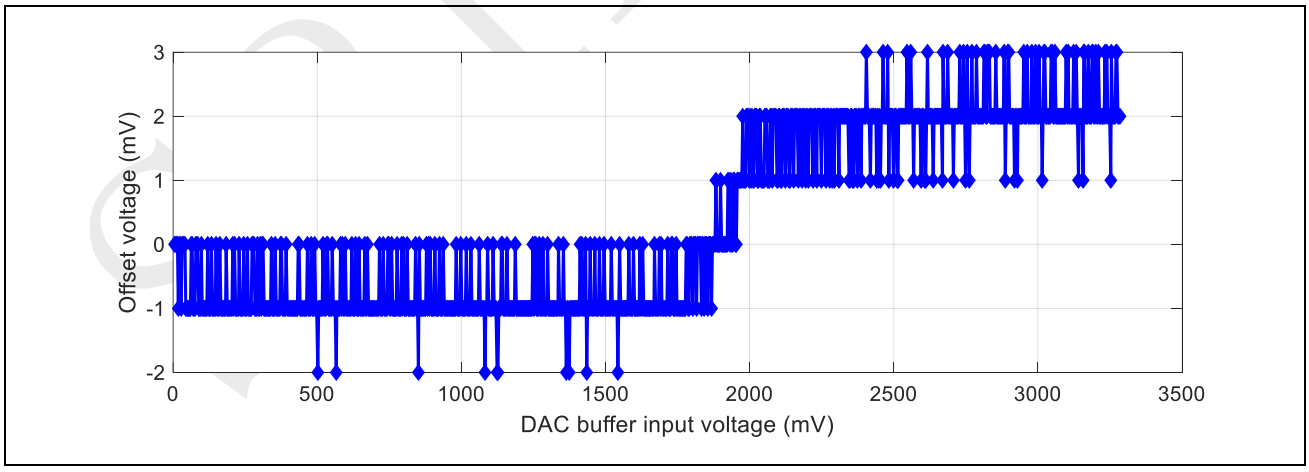
5.18 DAC buffer characteristics

Table 5-27: DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{out}	Output voltage range	-	0.3	-	V_{DVDD33}-0.4	V
t_{settle}[1]	Settling time	-	-	1	-	us
E_{offset}	Offset error	-	-	5	-	mV
C_L[1]	Capacitor load	-	-	-	50	pF
R_L[1]	Resistor load	-	5K	-	-	Ω

[1] Not subject to production test, guanranteed by design.

Figure 5-14: DAC buffer offset over Input voltage



5.19 D2S buffer characteristics

Table 5-28: D2S buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{out}	Output voltage range	-	0.3	-	V_{DVDD33}-0.3	V
t_{settle}	Settling time[1]	-	-	10	-	ms
E_{offset}	Offset error	-	-	10	-	mV
E_{gain}	Gain error	-	-	1	-	%
C_L	Capacitor load	-	-	1	-	uF
I_{on}	Current consumption	-	-	1	-	mA

[1] Settling time is measured by adding external RC filter, typical value is R=1kΩ, C=1uF.

5.20 Pre-Driver characteristics

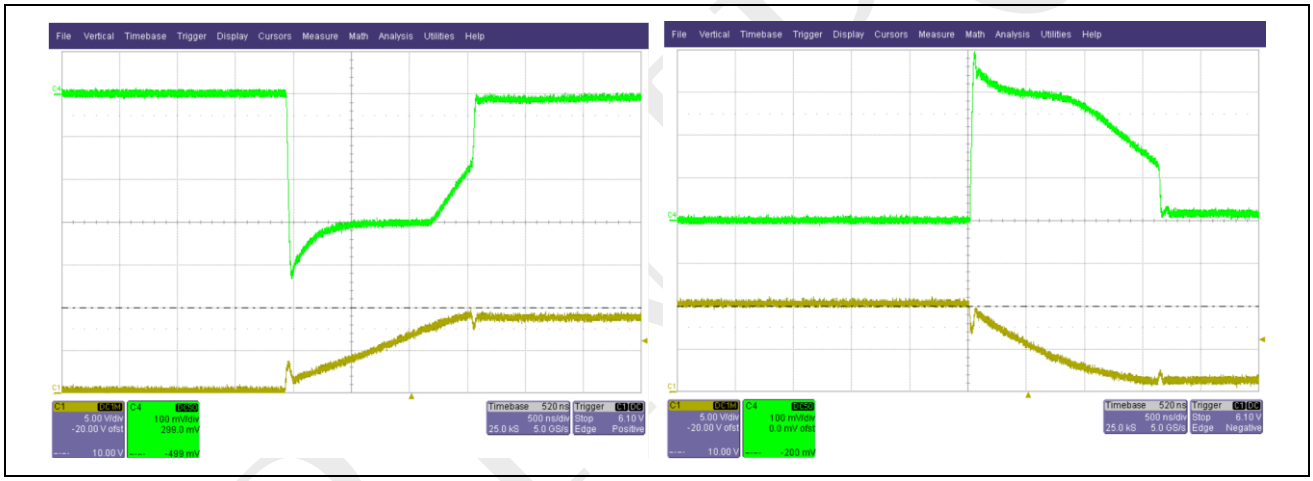
Table 5-29: Pre-Driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBATM}, V_{VBATCP}	Input supply voltage	-	5.5	-	28	V
	Extend supply range		28	-	40	V
OUTH-VPX	Pre-driver high side versus floating ground	VPX=VBAT Max driving capability	6.75[1]	9.4[1]	-	V
		VPX=0 Max driving capability	10[1]	10[1]	-	V
OUTL-GND	Pre-driver low side output, with respect to V_{GND}	VPX=VBAT Max driving capability	10[1]	10[1]	-	V
		VPX=0 Max driving capability	10[1]	10[1]	-	V
D_{MAX}	Maximum supported duty cycle		-	100	-	%
$t_{DL,MINC}$	Low-side propagation delay, min current strength code	1nF Capacitor as load	-	1150	-	ns
$t_{DH,MINC}$	High-side propagation delay, min current strength code	1nF Capacitor as load	-	1150	-	ns
$t_{DL,MAXC}$	Low-side propagation delay, max current strength code	1nF Capacitor as load	-	170	-	ns
$t_{DH,MAXC}$	High-side propagation delay, max current strength code	1nF Capacitor as load	-	170	-	ns
Δt	High/Low side delay mismatch	-	-	30	TBD	ns
$t_{r,MINC}$	Rise time, min code	1nF Capacitor as load	-	1100	-	ns
$t_{f,MINC}$	Fall time, min code	1nF Capacitor as load	-	900	-	ns
$t_{r,MAXC}$	Rise time, max code	1nF Capacitor as load	-	52	-	ns
$t_{f,MAXC}$	Fall time, max code	1nF Capacitor as load	-	48	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPX_{MIN}	High side return ground Minimum	Min voltage where high side signal still propagates	-10	-	-	V
V_{th,ds_mon}	Threshold for drain vs source voltage monitor	Threshold option = 1	0.24	0.3	0.36	V
$I_{Source\_Max\_HS}$	Source current - Charge current - High Side Driver	V_{VBATM} = V_{VBATCP} = 8V maximum strength	227	285	330	mA
$I_{Sink\_Max\_HS}$	Sink current - Discharge current-High Side Driver		237	294	345	mA
$I_{Source\_Max\_LS}$	Source current - Charge current - Low Side Driver		229	286	336	mA
$I_{Sink\_Max\_LS}$	Sink current - Discharge current-Low Side Driver		238	294	344	mA

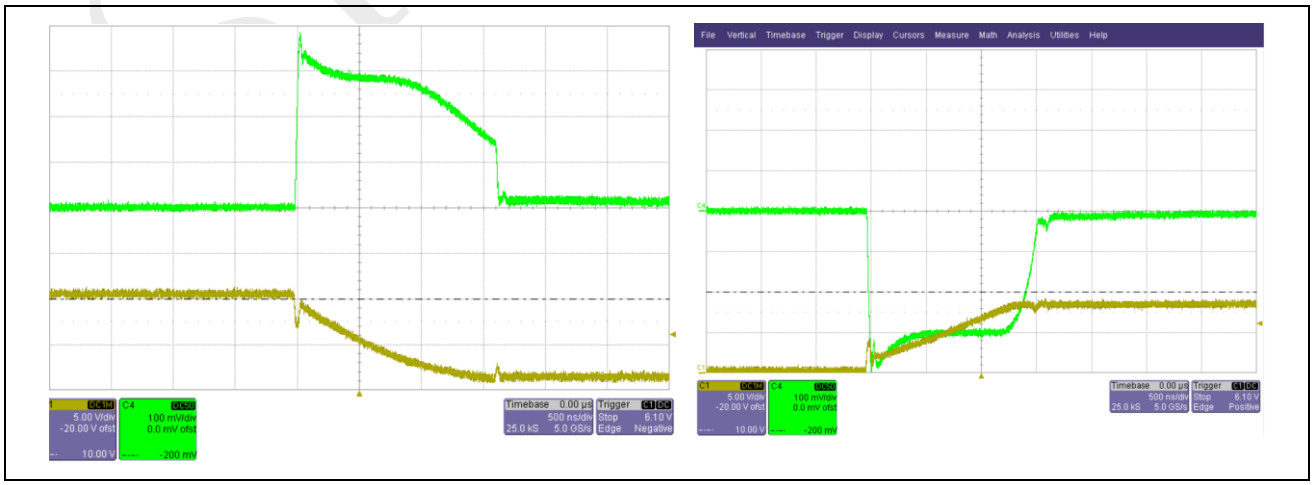
[1] Minimum value when V_{VBATM} = V_{VBATCP} = 5.5V. Typical value when V_{VBATM} = V_{VBATCP} = 12V.

Figure 5-15: Pre-Driver maximum sourcing/sinking current measurement (low side)



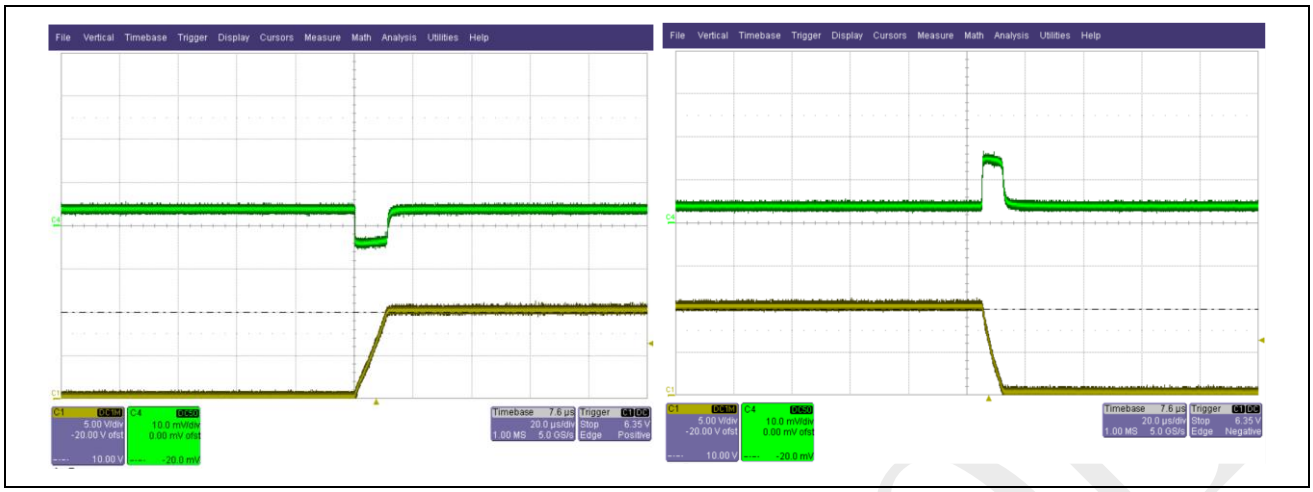
[1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 100mA/div).
[2] Pre-driver output charging 47nF capacitor.

Figure 5-16: Pre-Driver maximum sourcing/sinking current measurement (high side)



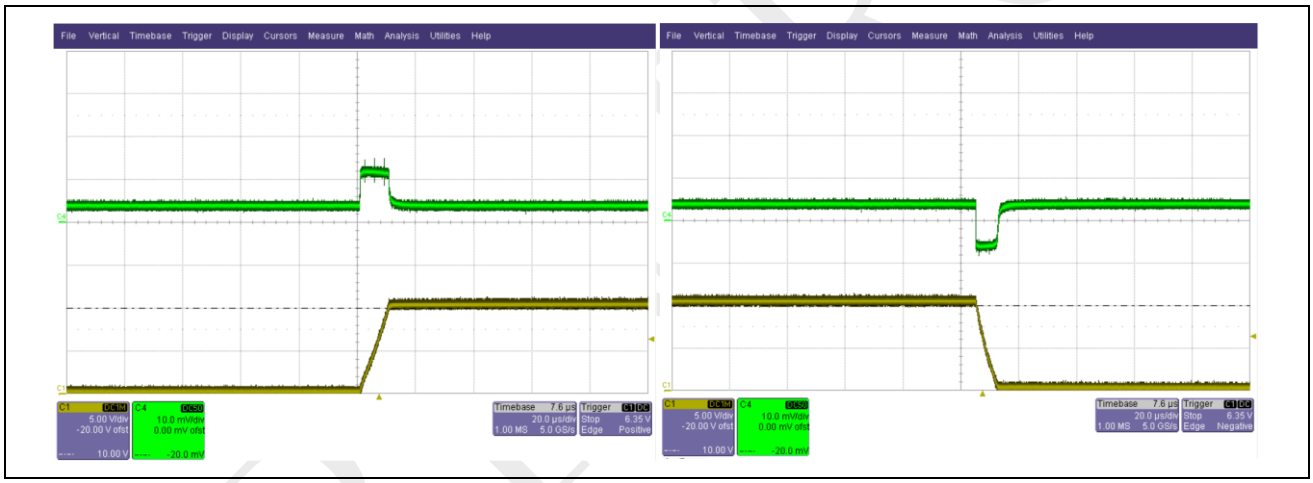
[1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 100mA/div).
[2] Pre-driver output discharging 47nF capacitor.

Figure 5-17: Pre-Driver minimum sourcing/sinking current measurement (low side)



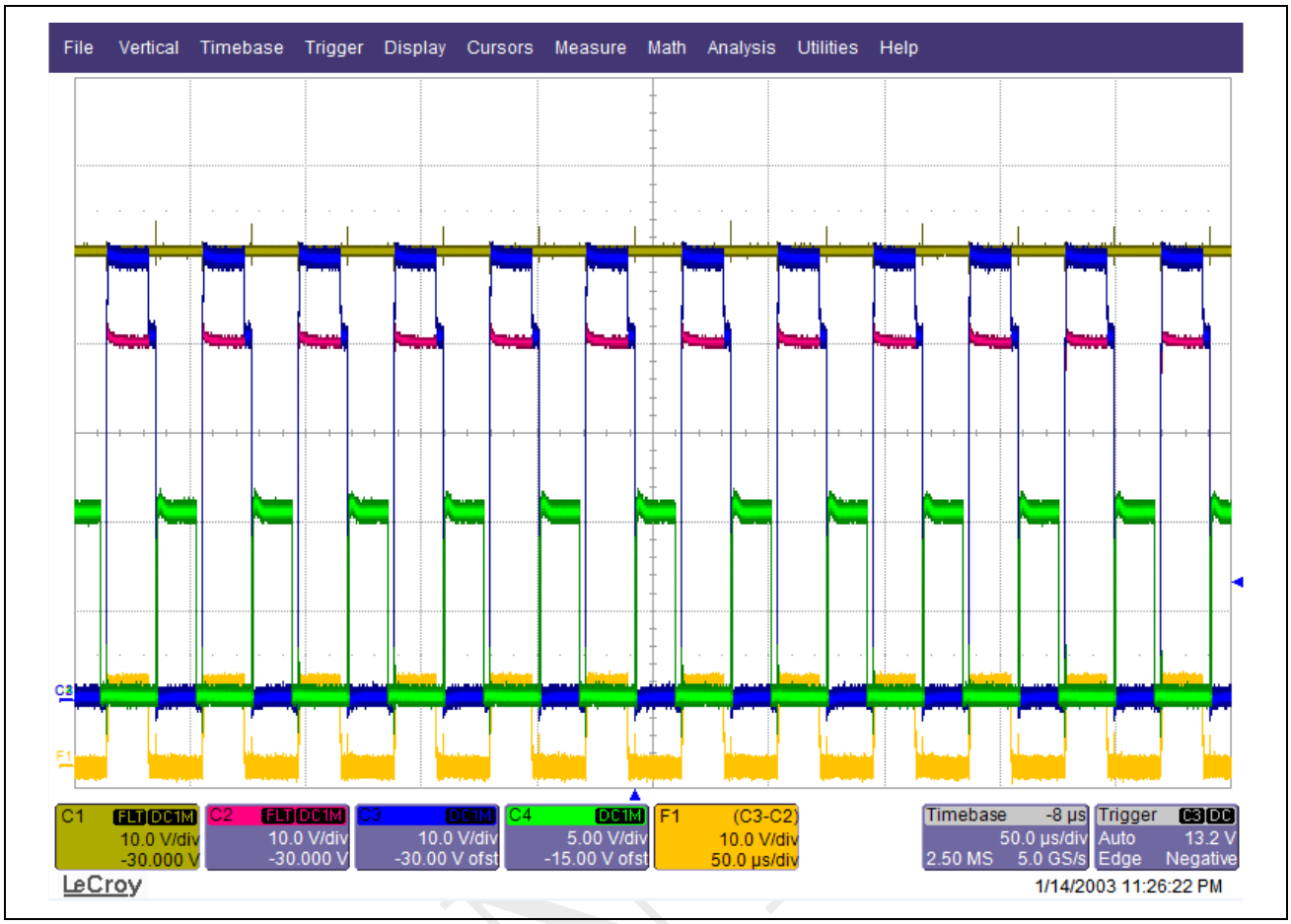
[1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 10mA/div).
[2] Pre-driver output discharging 10nF capacitor.

Figure 5-18: Pre-Driver minimum sourcing/sinking current measurement (high side)



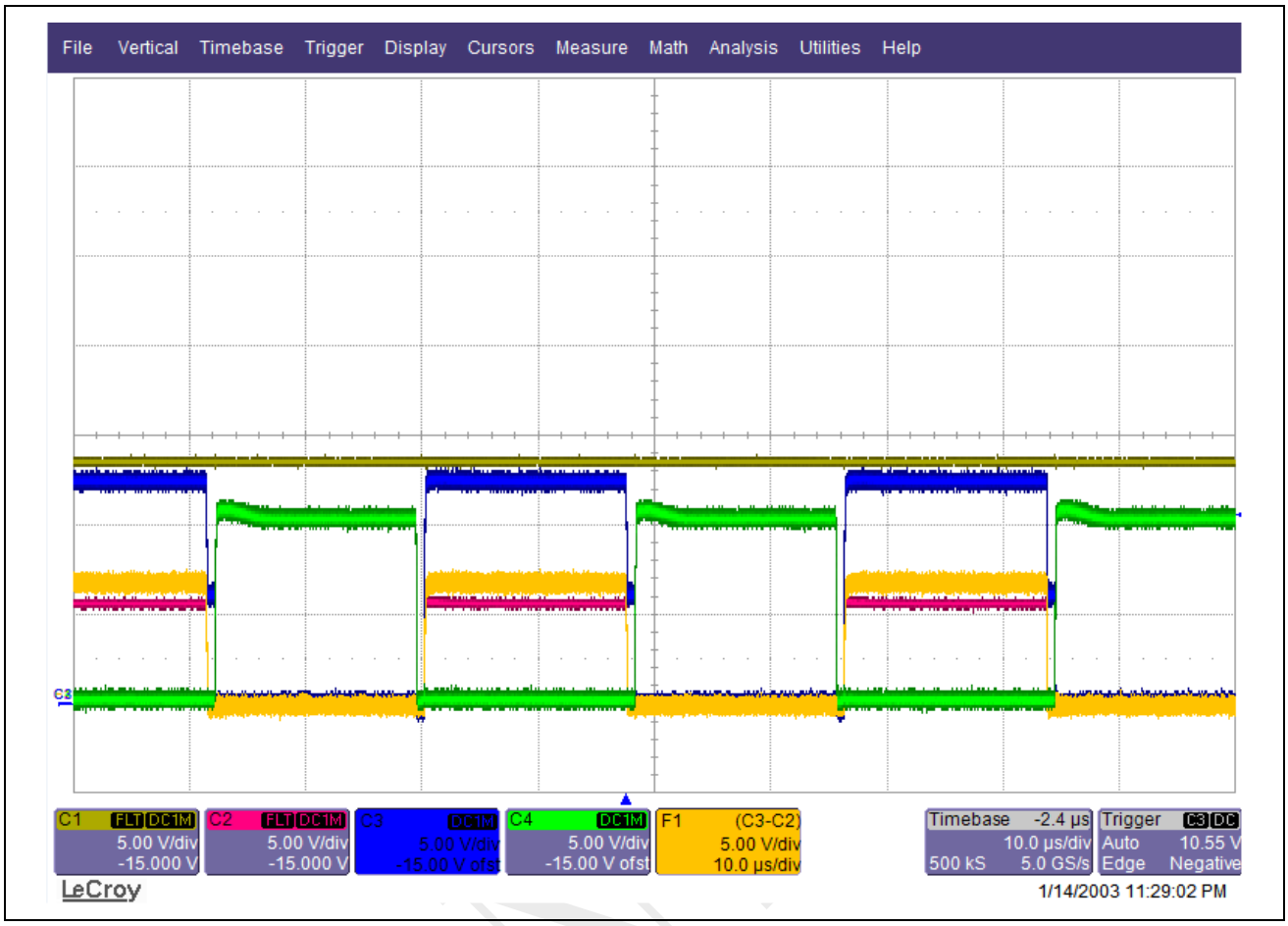
[1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 10mA/div).
[2] Pre-driver output discharging 10nF capacitor.

Figure 5-19: Pre-Driver toggling at V_{VBAT} =40V



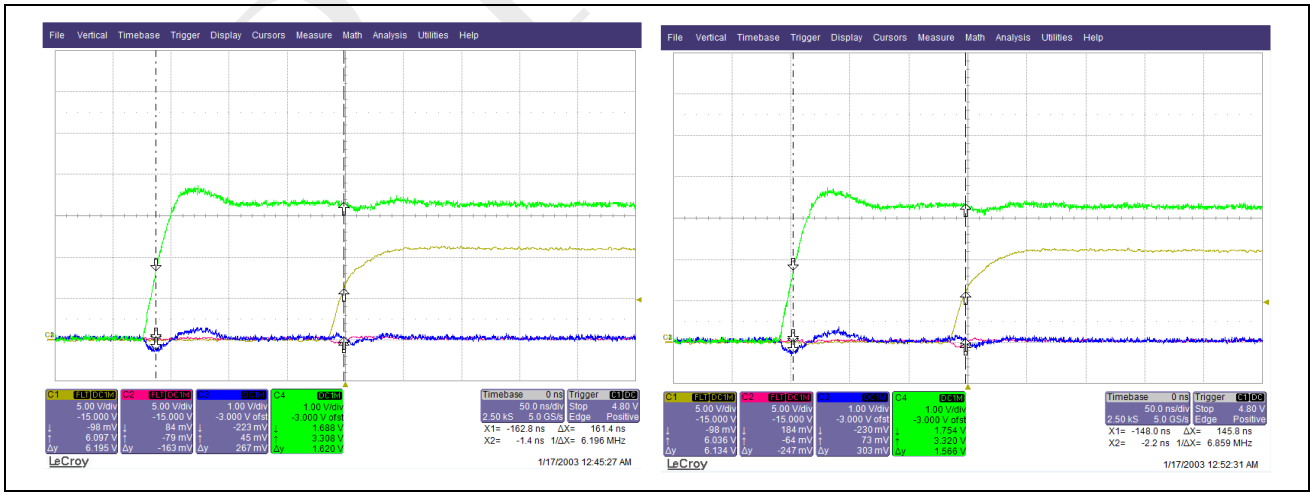
[1] C1 channel – VCP, C2 channel – VPX, C3 channel – high-side gate output (OUT_HS), C4 channel – low-side gate output (OUT_LS), Function channel – VPX subtracted from high-side gate output (VGS of high-side FET).

Figure 5-20: Pre-Driver toggling at V_{VBAT}=5.5V



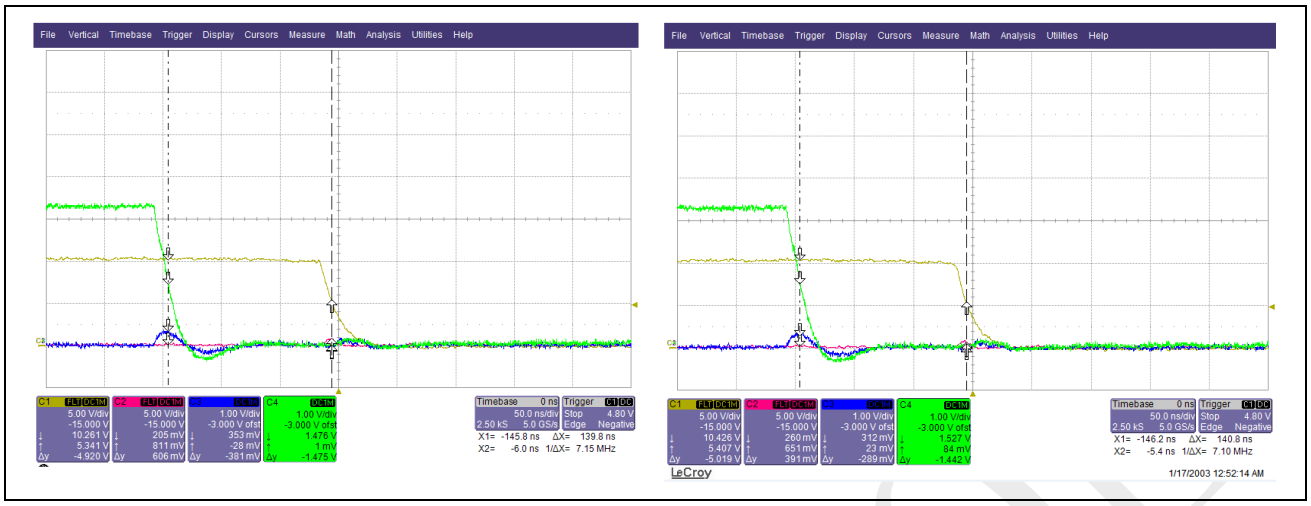
[1] C1 channel – VCP, C2 channel – VPX, C3 channel – high-side gate output (OUT_HS), C4 channel – low-side gate output (OUT_LS), Function channel – VPX subtracted from high-side gate output (VGS of high-side FET).

Figure 5-21: Low-side propagation delay measurements (rising edge)



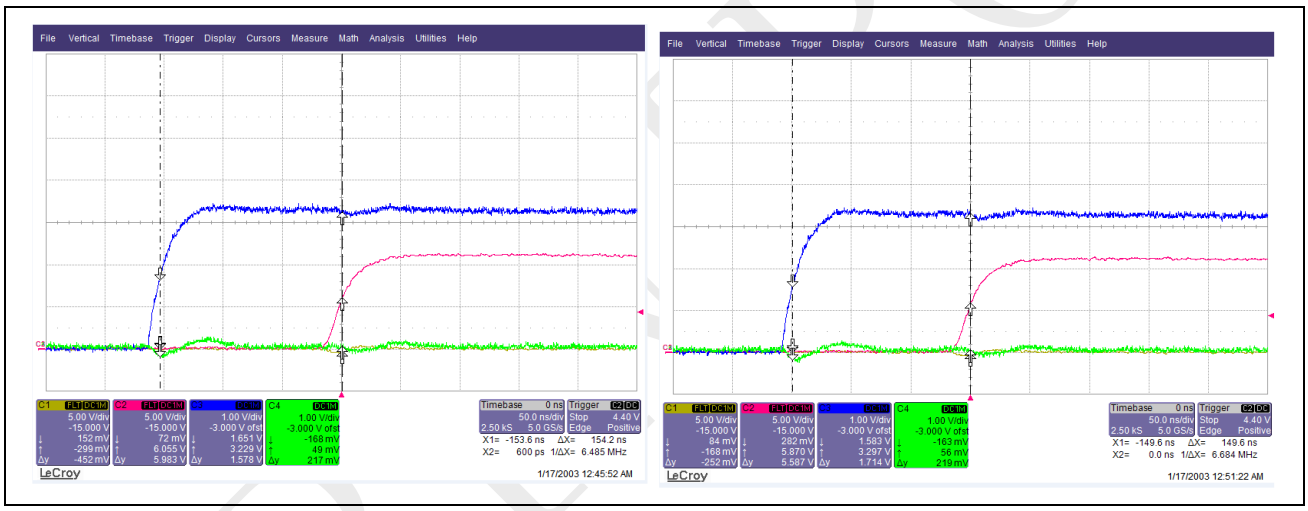
[1] VBAT=12V. C4 channel – PWM command; C1 channel – low-side gate output.

Figure 5-22: Low-side propagation delay measurements (falling edge)



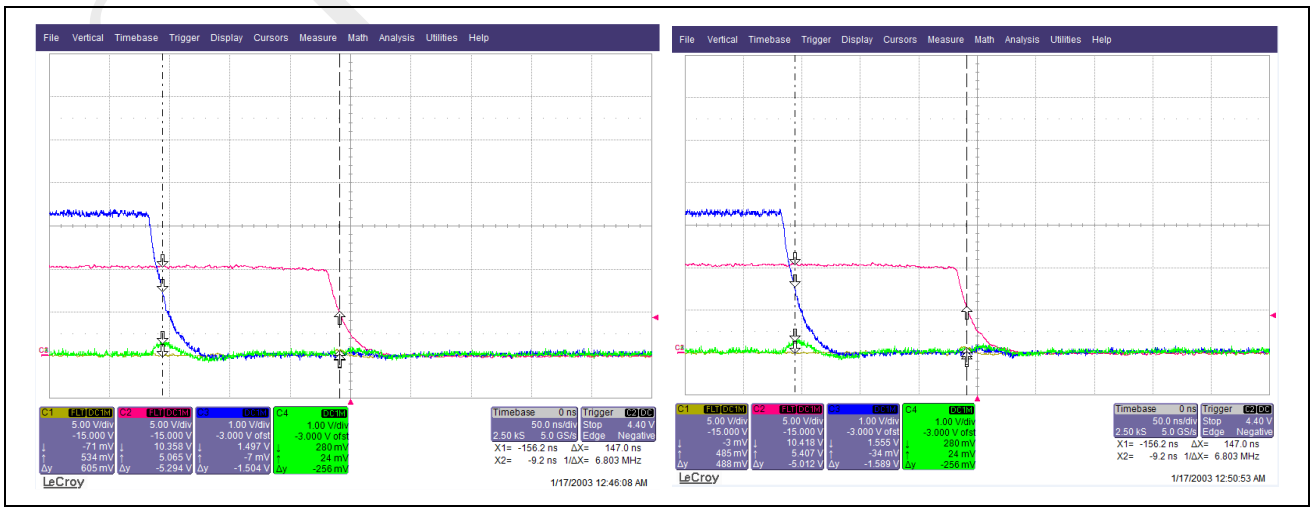
[1] VBAT=12V. C4 channel – PWM command; C1 channel – low-side gate output.

Figure 5-23: High-side propagation delay measurements (rising edge)



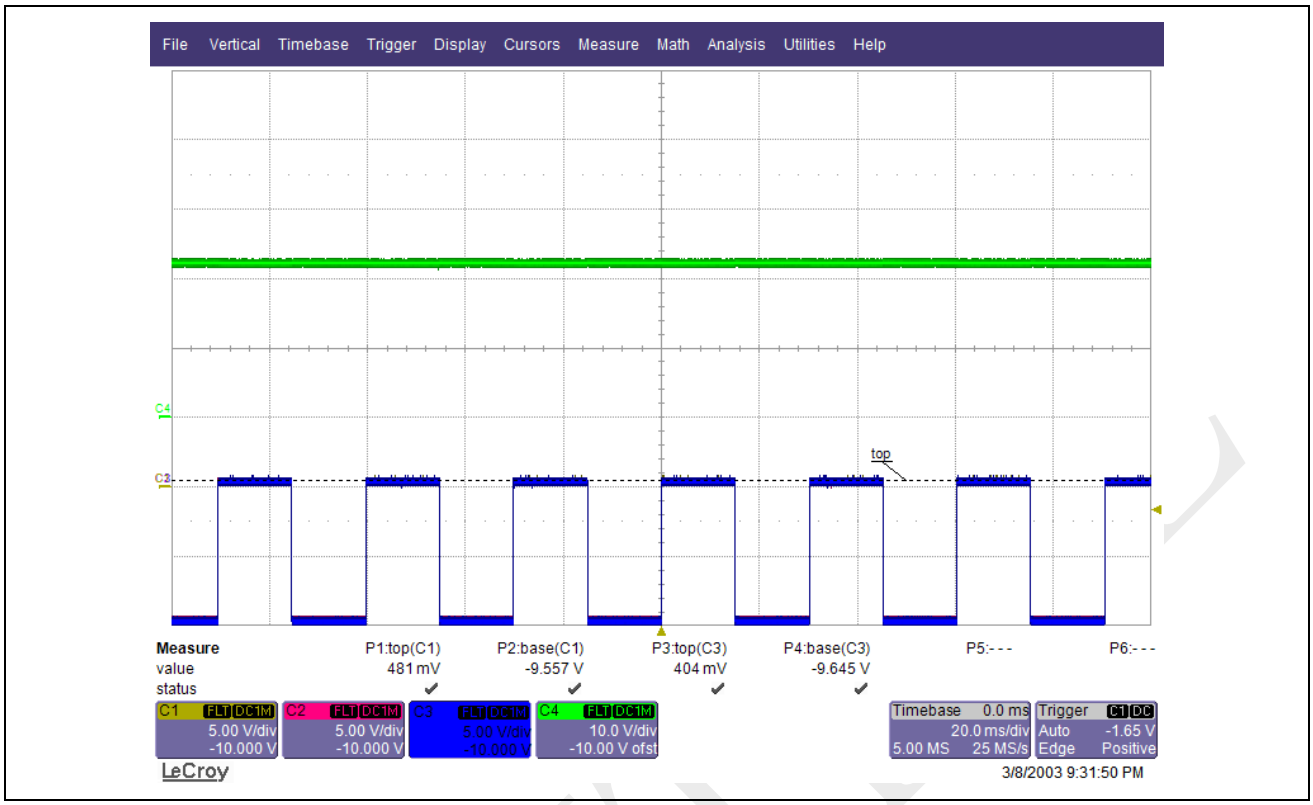
[1] VBAT=12V. C3 channel – PWM command; C2 channel – high-side gate output.

Figure 5-24: High-side propagation delay measurements (falling edge)



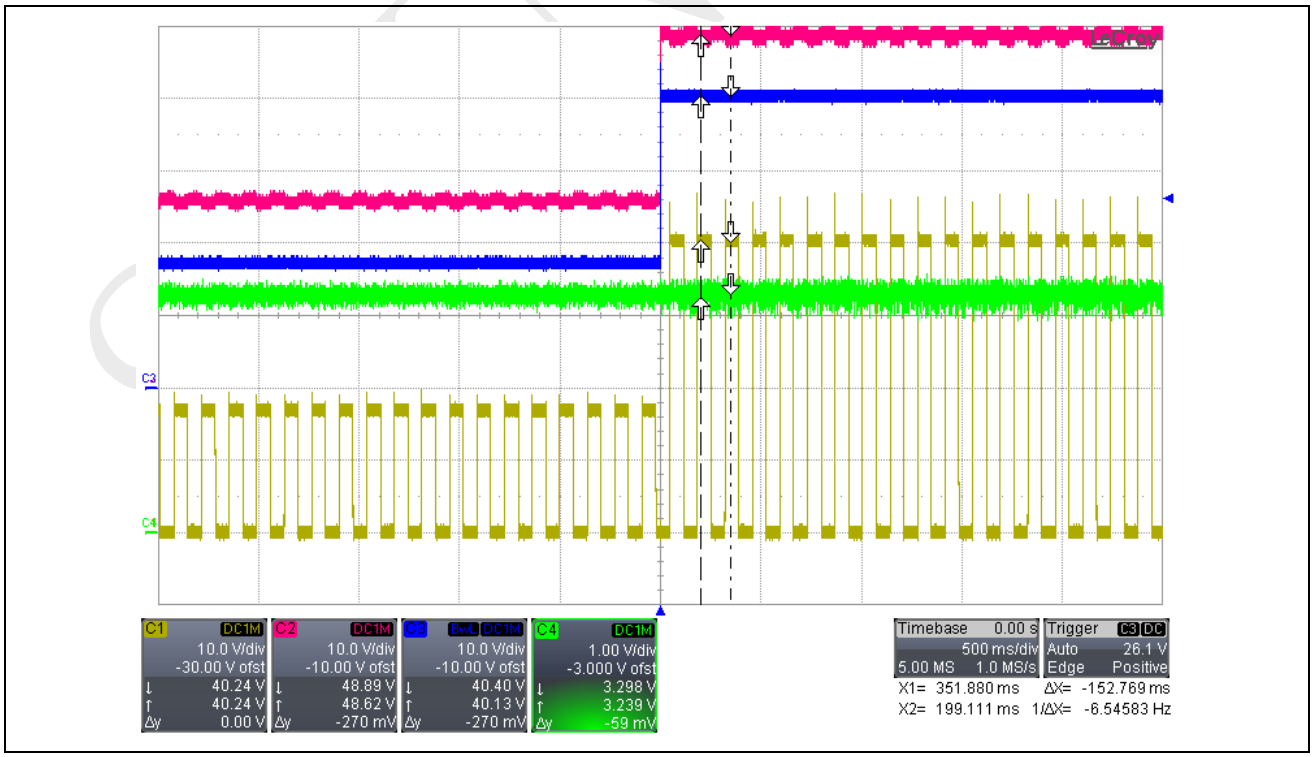
[1] VBAT=12V. C3 channel – PWM command; C2 channel – high-side gate output.

Figure 5-25: Demonstration of -10V support for all phases toggling in-phase



[1] C1/C2/C3 channel - high-side output for phases U/V/W toggling between -10V and approximately 0.5V; C4 channel - VCP.

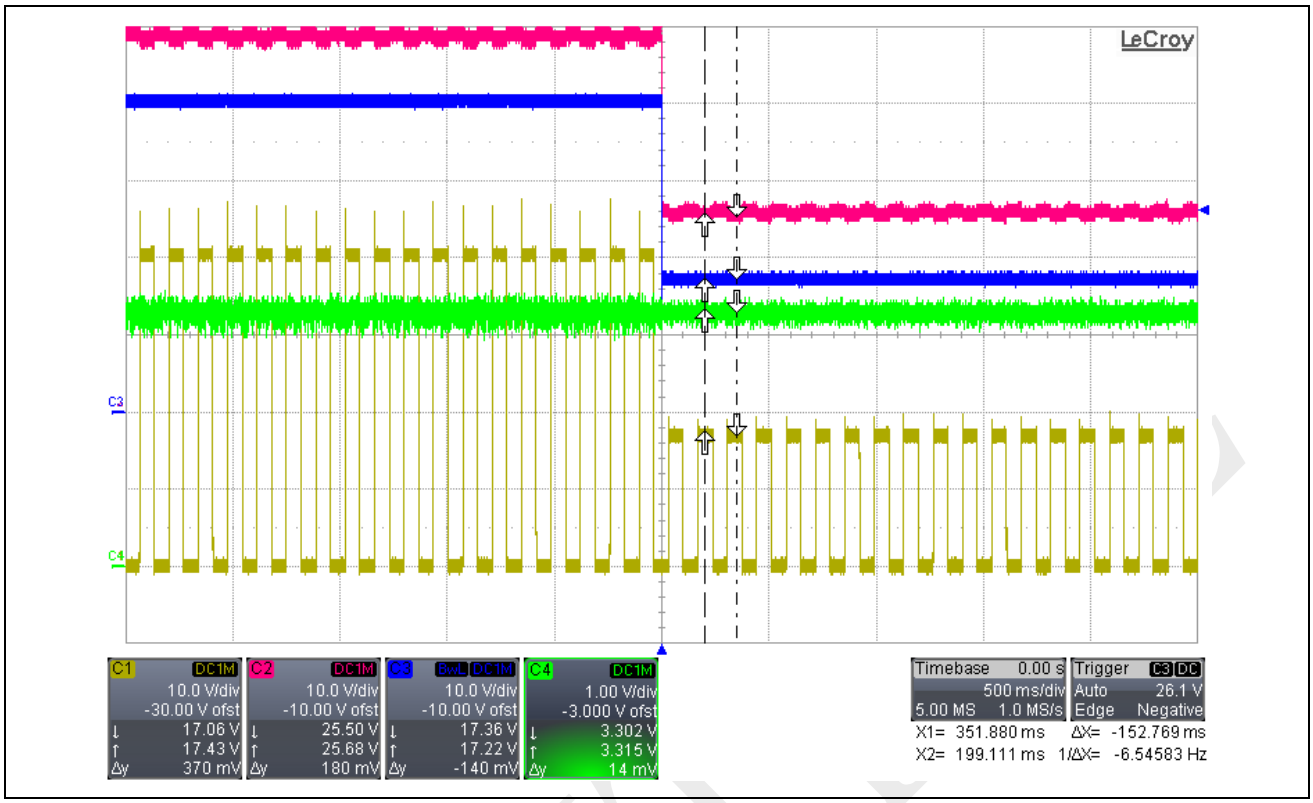
Figure 5-26: Pre-Driver system response during VBAT power step (from 17V to 40V)



[1] C1 channel - VPX, C2 channel - VCP, C3 channel - VBAT, C4 channel - DVDD.

[2] All phases are toggling in phase. The power is switched between 17V to 40V with 1.2MV/s slew rate.

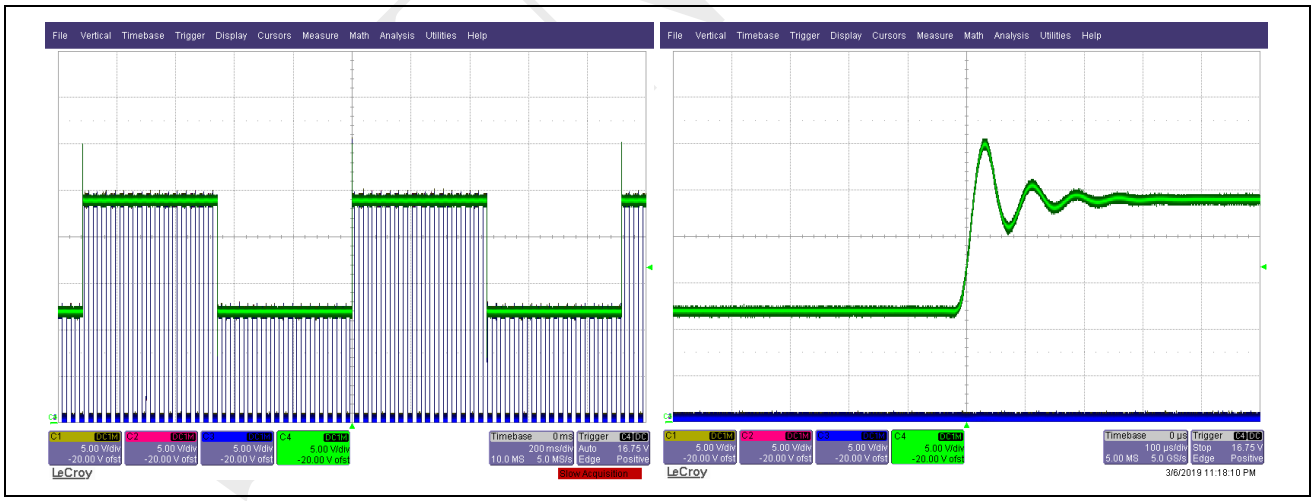
Figure 5-27: Pre-Driver system response during VBAT power step (from 40V to 17V)



[1] C1 channel - VPX, C2 channel - VCP, C3 channel - VBAT, C4 channel - DVDD.

[2] All phases are toggling in phase. The power is switched between 17V to 40V with 1.2MV/s slew rate.

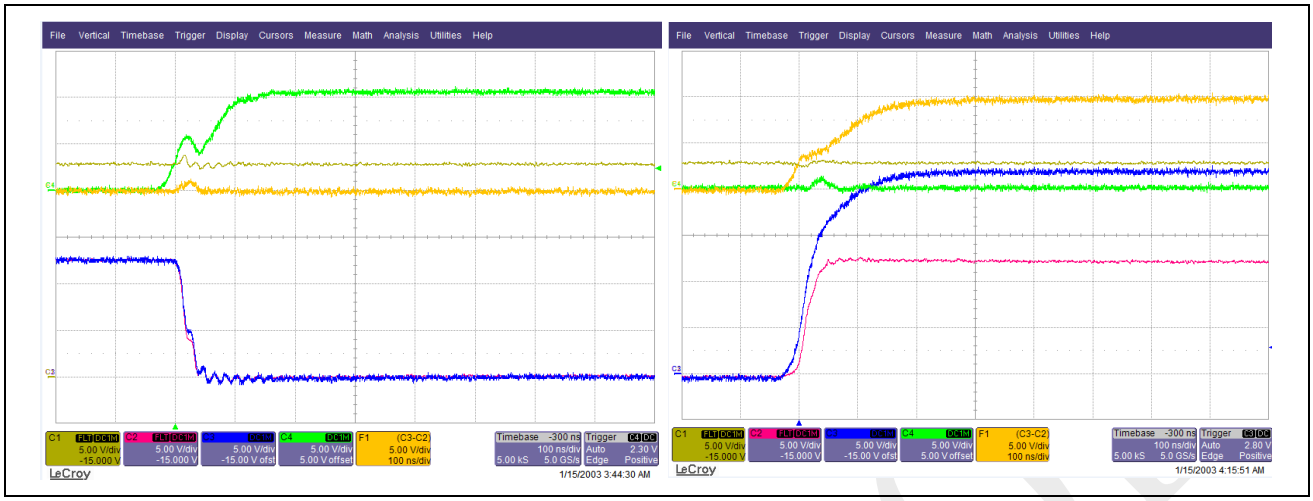
Figure 5-28: Pre-Driver system response during VBAT/VBATCP power step (from 12V to 24V)



[1] C1/2/3 channel – VPX_U/V/W, C4 channel - VBATCP.

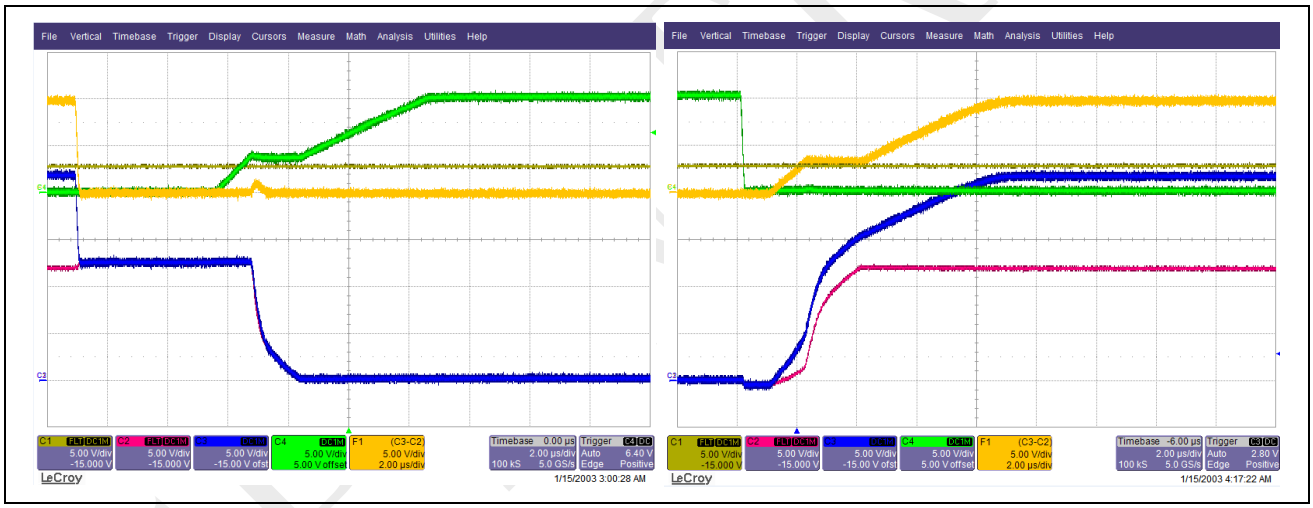
[2] All phases are toggling in phase. The power is switched between 12V to 24V with about 1MV/s slew rate.

Figure 5-29: H-bridge switching (using IRF640N FET's) when Pre-driver uses max current setting for each time segment



[1] C1 – VCP, C2 – VPX, C3 – OUT_HS, C4 – OUT_LS, F1 – OUT_HS-VPX, i.e. V_{GS} of high-side FET.

Figure 5-30: H-bridge switching (using IRF640N FET's) when Pre-driver uses min current setting for each time segment



[1] C1 – VCP, C2 – VPX, C3 – OUT_HS, C4 – OUT_LS, F1 – OUT_HS-VPX, i.e. V_{GS} of high-side FET.

5.21 LIN transceiver characteristics

Table 5-30: LIN receiver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
	Extend power supply range		28	-	40	V
V_{BUS_REC}	Receiver recessive state	LIN SPEC 2.2 (Par. 18)	0.6	-	-	V_{VBAT}
V_{BUS_DOM}	Receiver dominant state	LIN SPEC 2.2 (Par. 17)	-	-	0.4	V_{VBAT}
V_{BUS_CNT}	Receiver center voltage	LIN SPEC 2.2 (Par. 19)	0.475	0.5	0.525	V_{VBAT}
V_{HYS}	Receiver hysteresis	LIN SPEC 2.2 (Par. 20)	0.07	0.12	0.175	V_{VBAT}
$t_{RX\_PD(L)}$	Propagation delay bus dominant to RxD LOW	LIN Spec 2.2 (Par. 31)	0.1	-	6.0	us
$t_{RX\_PD(H)}$	Propagation delay bus recessive to RxD HIGH	LIN Spec 2.2 (Par. 31)	0.1	-	6.0	us
t_{RX_SYM}	Receiver delay symmetry	$t_{RX\_SYM} = t_{RX\_PD(L)} - t_{RX\_PD(H)}$ LIN Spec 2.2 (Par. 32)	-2.0	-	2.0	us

Table 5-31: LIN wake-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
	Extend power supply range		28	-	40	V
V_{TH_WK}	Wake-up threshold	T_J = -40 ~ 150 °C	0.475	0.52	0.55	V_{VBAT}
$V_{TH\_WK\_HYST}$	Wake-up hysteresis	T_J = -40 ~ 150 °C	0.04	0.07	0.10	V_{VBAT}
$t_{WK\_FILT\_ANA}$[1]	Wake-up filter time (internal analog filter delay)	-	-	3.83	-	us

[1] The total dominant time for LIN wake-up is $t_{WK\_FILT\_ANA}$ plus digital filter time (>100us).

Table 5-32: LIN transmitter characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
	Extend power supply range	-	28	-	40	V
$V_{BUS\_REC\_OUT}$	Bus recessive output voltage	5.5V ≤ V_{VBAT} ≤ 28V	0.8	-	-	V_{VBAT}
$V_{BUS\_DOM\_OUT}$	Bus dominant output voltage	7V ≤ V_{VBAT} ≤ 28V	-	-	0.2	V_{VBAT}
		5.5V ≤ V_{VBAT} < 7V	-	-	0.223	V_{VBAT}
I_{BUS_LIM}	Bus short circuit current	LIN Spec 2.2 (Par. 12)	40.0	-	150.0	mA
$t_{BUS\_Short\_filt}$	Bus short circuit filter time	-	-	9	-	us
$I_{BUS\_NO\_GND}$[1]	Leakage current (loss of ground)	LIN Spec 2.2 (Par. 15)	-1000	-425.8	1000	uA
$I_{BUS\_NO\_BAT}$	Leakage current	LIN Spec 2.2 (Par. 16)	-	9.36	20.0	uA
$I_{BUS\_PAS\_dom}$	Leakage current	LIN Spec 2.2 (Par. 13)	-1.0	-0.545	-	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{BUS\_PAS\_rec}$	Leakage current	LIN Spec 2.2 (Par. 14)	-	6.23	20.0	uA
R_{slave}	Bus pull-up resistance	LIN Spec 2.2 (Par. 26)	20.0	32.3	47.0	kΩ
D1[2]	Duty cycle D1 Normal Slope Mode (for worst case at 20 kbit/s)	LIN Spec 2.2 (Par. 27) 1K pull-up resistor 1nF load cap or 0.5K pull-up resistor 10nF load cap	0.396	-	-	-
D2[3]	Duty cycle D2 Normal Slope Mode (for worst case at 20 kbit/s)	LIN Spec 2.2 (Par. 28) 1K pull-up resistor 1nF load cap or 0.5K pull-up resistor 10nF load cap	-	-	0.581	-
D3[4]	Duty cycle D3 (for worst case at 10.4 kbit/s)	LIN Spec 2.2 (Par. 29) 1K pull-up resistor 1nF load cap or 0.5K pull-up resistor 10nF load cap	0.417	-	-	-
D4[5]	Duty cycle D4 (for worst case at 10.4 kbit/s)	LIN Spec 2.2 (Par. 30) 1K pull-up resistor 1nF load cap or 0.5K pull-up resistor 10nF load cap	-	-	0.590	-
D5[1][6][8]	Duty cycle D5 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	0.5K pull-up resistor 1nF load cap	0.390	-	-	-
D6[1][7][8]	Duty cycle D6 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	0.5K pull-up resistor 1nF load cap	-	-	0.610	-
C_{LIN_IN}	LIN input capacity	-	-	15	30.0	pF
$t_{timeout}$	TxD dominant time out	V_{TxD} = 0 V	-	12.4	-	ms
T_{j_SD}[1]	Thermal shutdown temp	-	140	160	180	°C
DT[1]	Thermal shutdown hysteresis	-	-	10	-	°C

[1] Not subject to production test, guaranteed by design.
[2] THRec(max) = 0.744 ×VS; THDom(max) = 0.581 ×VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 50 µs; D1 = tbus_rec(min)/2 tbit;
[3] THRec(min) = 0.422 ×VS; THDom(min) = 0.284 ×VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 50 µs; D1 = tbus_rec(max)/2 tbit;
[4] THRec(max) = 0.778 ×VS; THDom(max) = 0.616 ×VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 96 µs; D1 = tbus_rec(min)/2 tbit;
[5] THRec(min) = 0.389 ×VS; THDom(min) = 0.251 ×VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 96 µs; D1 = tbus_rec(max)/2 tbit;
[6] THRec(max) = 0.744 ×VS; THDom(max) = 0.581 ×VS; V_{VBAT} = 13.5 V; tbit = 8.7 µs; D1 = tbus_rec(min)/2 tbit;
[7] THRec(min) = 0.422 ×VS; THDom(min) = 0.284 ×VS; V_{VBAT} = 13.5 V; tbit = 8.7 µs; D1 = tbus_rec(max)/2 tbit.
[8] D5~D6 bus load condition is 0.5K pull-up resistor and 1nF load cap.

5.22 SPI characteristics

Table 5-33: SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	-	-	-	50	MHz
$t_{SCLK(H)}$	SCLK clock high time	-	10	-	-	ns
$t_{SCLK(L)}$	SCLK clock low time	-	10	-	-	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(MO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(MI)}$	Data input setup time	-	6	-	-	ns
$t_{H(MI)}$	Data input hold time	-	2	-	-	ns
SPI slave mode						
$t_{SU(SFRM)}$	SFRM enable setup time	-	5.6	-	-	ns
$t_{H(SFRM)}$	SFRM enable hold time	-	1.5	-	-	ns
$t_{A(SO)}$	Data output access time	-	4	-	10	ns
$t_{DIS(SO)}$	Data output disable time	-	4	-	10	ns
$t_{V(SO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(SO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(SI)}$	Data input setup time	-	6	-	-	ns
$t_{H(SI)}$	Data input hold time	-	2	-	-	ns

5.23 MON characteristics

Table 5-34: MON characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
	Extend power supply range	-	28	-	40	V
V_{TH}[1]	Wake-up/monitoring threshold voltage	-	0.48	0.50	0.53	V_{VBAT}
V_{TH_HYST}[1]	Threshold hysteresis	-	0.04	0.065	0.08	V_{VBAT}
I_{PU}	Pull-up current	0.4 * V_{VBAT}	-20	-10	-1	uA
I_{PD}	Pull-down current	0.6 * V_{VBAT}	1	10	20	uA
I_{IK}	Input leakage current	0V < V_{MON} < 28V 5.5V < V_{VBAT}< 28V	-2	-	2	uA
I_{on}	Operation current	T_J = -40 ~ 150 °C	-	1.7	4	uA
I_{off}[2]	Off current	-	-	10	300	nA
$t_{WK\_FILT\_ANA}$[3]	Wake-up filter time (internal analog filter delay)	-	-	3.55	-	us

[1] Without external serial resistor Rs (with Rs: ΔV = IPD * Rs or ΔV=IPU*Rs).
[2] Not subject to production test, guaranteed by design.
[3] The minimal time for MON wake-up is $t_{WK\_FILT\_ANA}$ plus digital filter time (>50us).

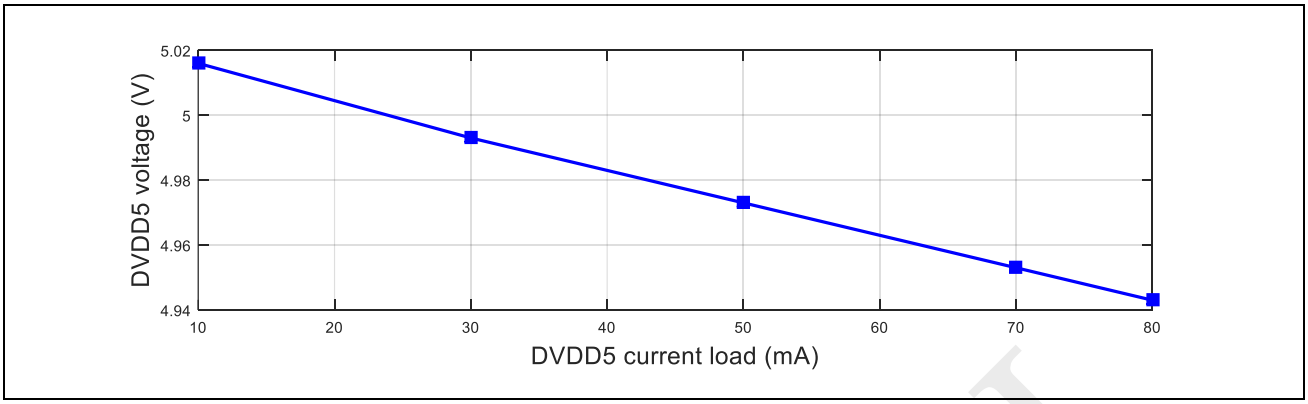
5.24 DVDD5 characteristics

Table 5-35: DVDD5 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
	Extend power supply range	-	28	-	40	V
C_{load}[1]	Load capacitor	-	2.2	-	4.7	uF
I_{load}	Load current @ active mode	-	-	-	80	mA
V_{out_trim}	Trim step @ active mode	-	-	66.67	-	mV
V_{out}	Output voltage @ active mode	-	-	5	-	V
d_{V_load}	Load regulation @ active mode	-	-	68	250	mV
I_{oc}	Overcurrent threshold @ active mode	-	81	151	312	mA
V_{out}[2]	Output voltage @ stop mode	-	-	4.45	-	V
$I_{load,stop}$[2]	Drive capability (stop mode)	V_{BAT}=5.5V	-	8	-	mA
		V_{BAT}=40V	-	16	-	mA

[1] Not subject to production test, guaranteed by design.
[2] Only drive internal loading.

Figure 5-31: DVDD5 load regulation



5.25 DVDD33 characteristics

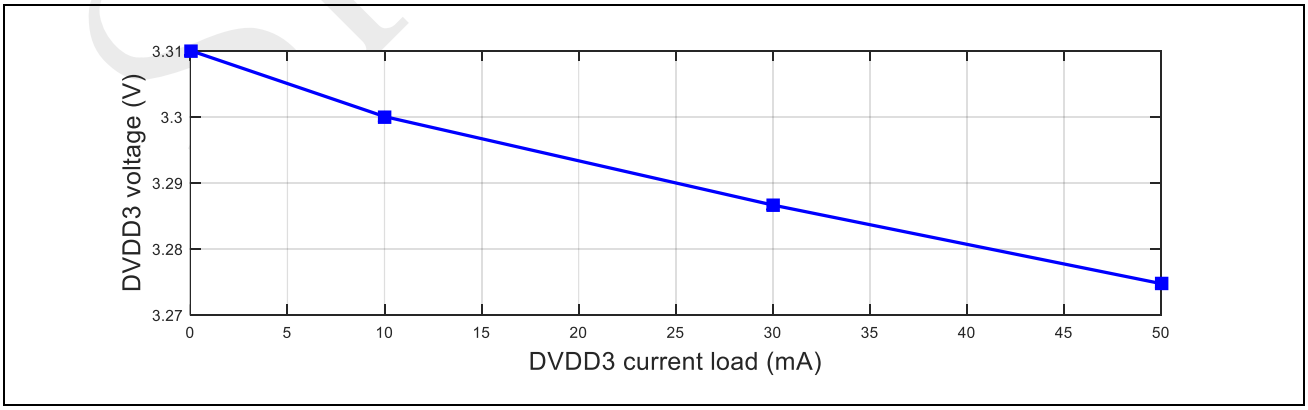
Table 5-36: DVDD33 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
	Extend power supply range	-	28	-	40	V
C_{load}[1]	Load capacitor	-	2.2	-	4.7	uF
I_{load}	Load current @ active mode	-	-	-	50	mA
V_{out_trim}	Trim step @ active mode	-	-	44	-	mV
V_{out}	Output voltage @ active mode	-	-	3.3	-	V
d_{V_load}	Load regulation @ active mode	-	-	38.65	66	mV
I_{oc}	Overcurrent threshold @ active mode	-	53	100	211	mA
V_{out}[2]	Output voltage @ stop mode	-	-	2.88	-	V
$I_{load,stop}$[2]	Drive capability (stop mode)	-	2.57	4.05	6.57	mA

[1] Not subject to production test, guaranteed by design.

[2] Only internal current.

Figure 5-32: DVDD33 load regulation



5.26 VCAP12 characteristics

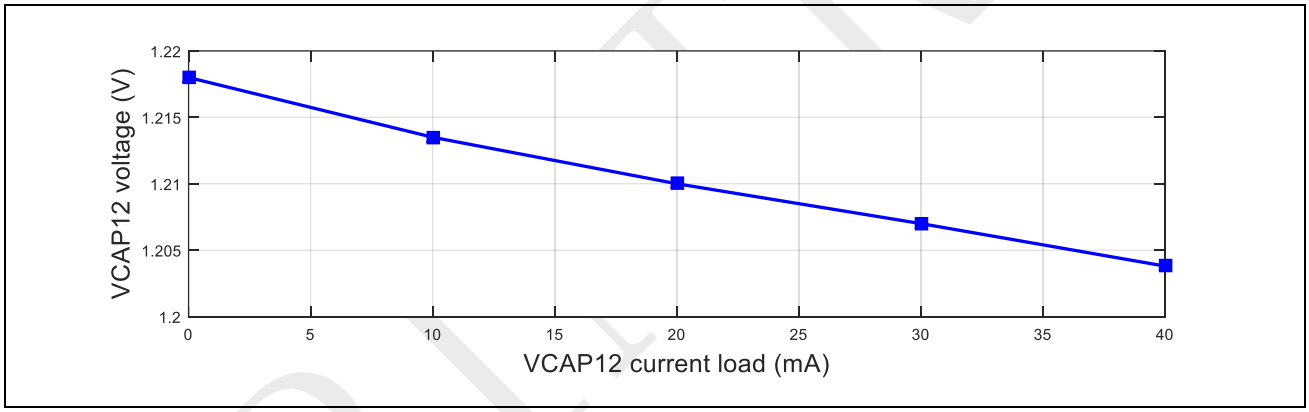
Table 5-37: VCAP12 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
	Extend power supply range	-	28	-	40	V
C_{load}[1]	Load capacitor	-	1	2.2	4.7	uF
I_{load}	Load current @ active mode	-	-	-	40	mA
V_{out_trim}	Trim step @ active mode	-	-	20	-	mV
V_{out}	Output voltage @ active mode	-	-	1.2	-	V
d_{V_load}	Load regulation @ active mode	-	-	14	40	mV
I_{oc}	Overcurrent threshold @ active mode	-	60	81.5	107	mA
V_{out}[2]	Output voltage @ stop mode	-	-	1.025	-	V

[1] Not subject to production test, guaranteed by design.

[2] Only internal current.

Figure 5-33: VCAP12 load regulation



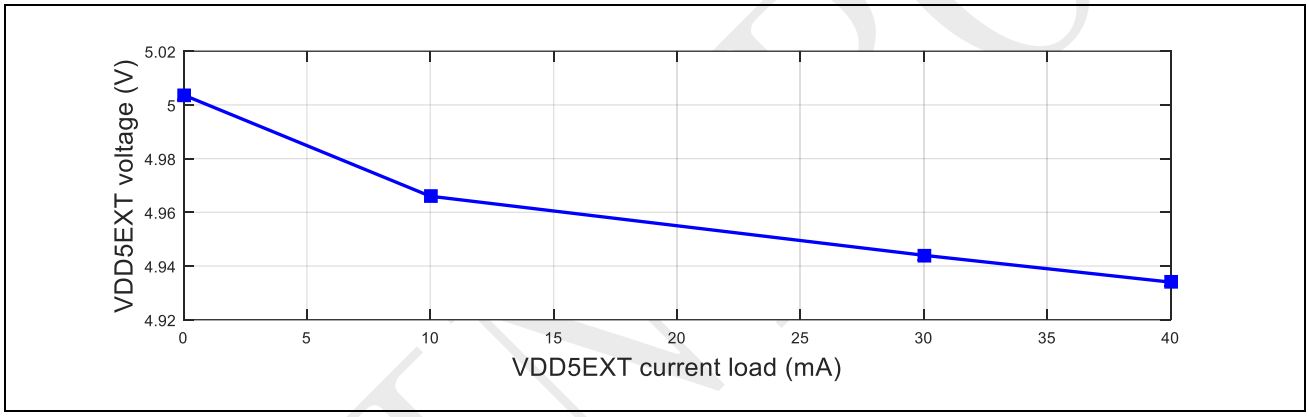
5.27 DVDD5EXT characteristics

Table 5-38: DVDD5EXT characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	-	5.5	-	28	V
C_{load}[1]	Load capacitor	-	1	2.2	4.7	uF
I_{load}	Load current @ active mode	-	-	-	40	mA
V_{out_trim}	Trim step @ active mode	-	-	66.67	-	mV
V_{out}	Output voltage @ active mode	-	-	5	-	V
d_{V_load}	Load regulation @ active mode	-	-	69.7	123	mV
I_{oc}	Overcurrent threshold @ active mode	-	45	77.33	170	mA

[1] Not subject to production test, guaranteed by design.

Figure 5-34: DVDD5EXT load regulation



5.28 Flash memory characteristics

The characteristics are given at T_J = -40 to 150 °C unless otherwise specified.

Table 5-39: Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RD}	Read access time	-	35	-	ns
t_{PROG}	Word (64-bit) program time	-	8	10	us
t_{SE}	Sector erase time	-	3.2	4	ms
t_{CE}	Chip erase time	-	16	20	ms
N_{END}	Endurance (erase/program cycle)	T_J = 85 °C	100000	-	cycles
t_{RET}	Data retention duration	T_J = 85 °C	20	-	years

5.29 Electrical sensitivity characteristics

Table 5-40: ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C	LIN Pin	8000	V
			VBAT Pin VBATM Pin VBATCP Pin MON Pin	4000	V
			Other Pins	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	-	500	V
			Corner Pins	750	V

Table 5-41: Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 125 °C V_{VBAT}=V_{VBATM}=V_{VBATCP}=40V, V_{DVDD5} = 5.5V, V_{DVDD33} = 3.63V, V_{VCAP12} = 1.32V	100	mA

5.30 Moisture Sensitivity Level characteristics

Table 5-42: Thermal resistance characteristics（QFN48 package）

Symbol	Parameter	Conditions	Max	Unit
MSL	Moisture Sensitivity Level	-	3	-

5.31 Thermal resistance characteristics

Table 5-43: Thermal resistance characteristics（QFN48 package）

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	-	5.4751	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	2-layer PCB[1] PCB Copper content (Top layer = 60%, Bottom layer = 80%)	28.0204	°C/W

[1] The size of PCB test board is 110mm x 110mm x 1.6mm.

Table 5-44: Thermal resistance characteristics（QFN56 package）

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	-	6.5942	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	4-layer PCB[1] PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	27.9046	°C/W

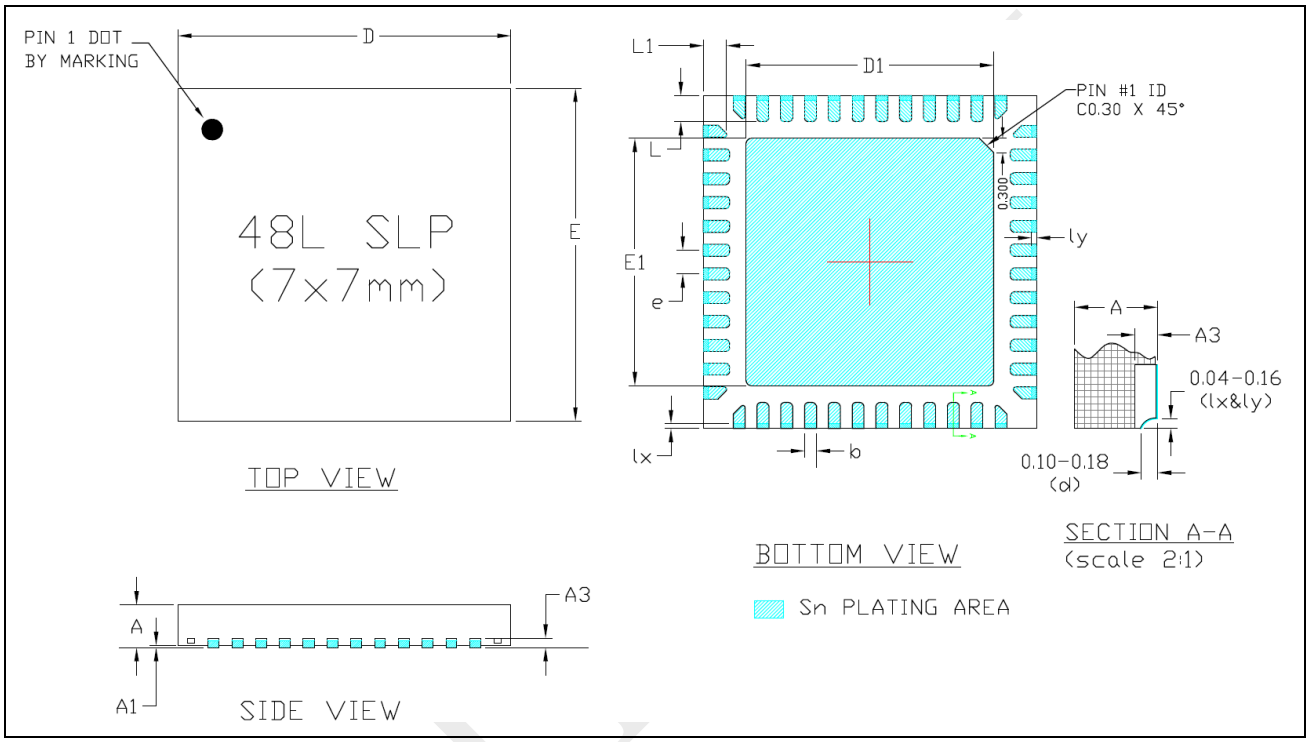
[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

6 Package information

The package type of SPD1179/SPD1176 is 48-pin Wettable Flank QFN or 56-pin QFN. The detail information is as follows:

6.1 QFN48 (Wettable Flank)

Figure 6-1: QFN48 - 48 pin, 7 x 7 mm wettable flank quad flat no-lead package outline

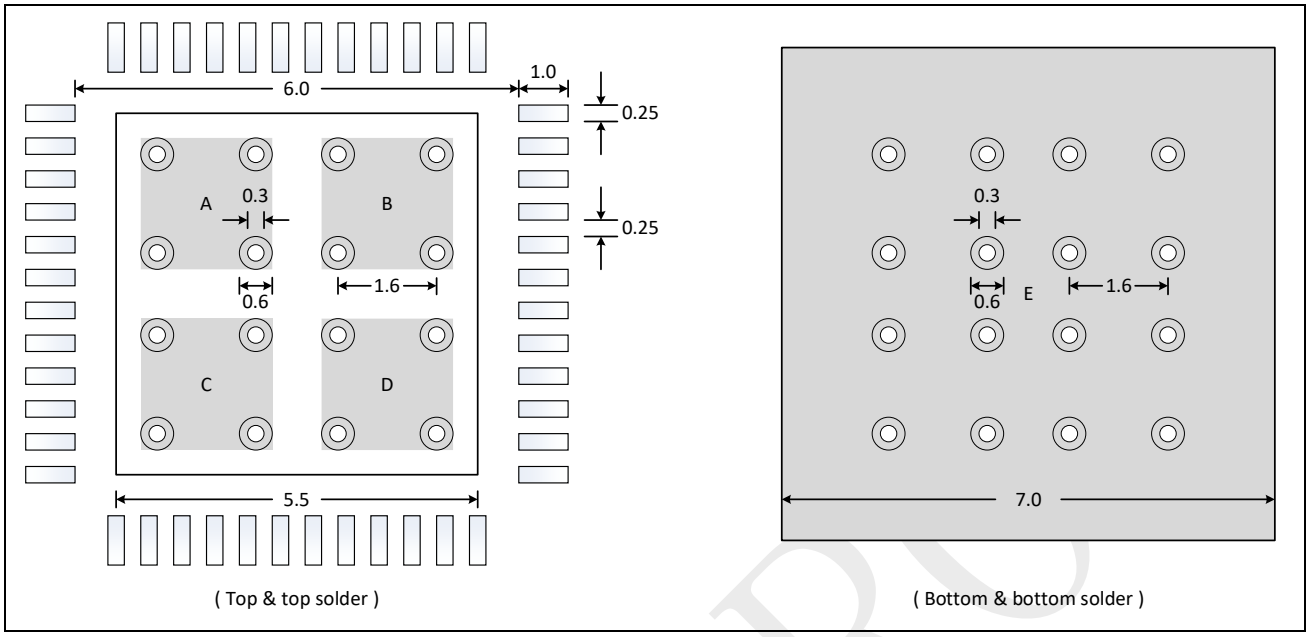


[1] Drawing is not to scale.

Table 6-1: QFN48 – 48 pin, 7 x 7 mm wettable flank quad flat no-lead package mechanical data

Symbol	Millimeter		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3	0.203REF		
D	6.95	7.00	7.05
E	6.95	7.00	7.05
D1	5.15	5.20	5.25
E1	5.15	5.20	5.25
b	0.20	0.25	0.30
L	0.50	0.55	0.60
L1	0.43	0.48	0.53
e	0.50BSC		

Figure 6-2: QFN48 - 48 pin, 7 x 7 mm wettable flank quad flat no-lead package recommended footprint

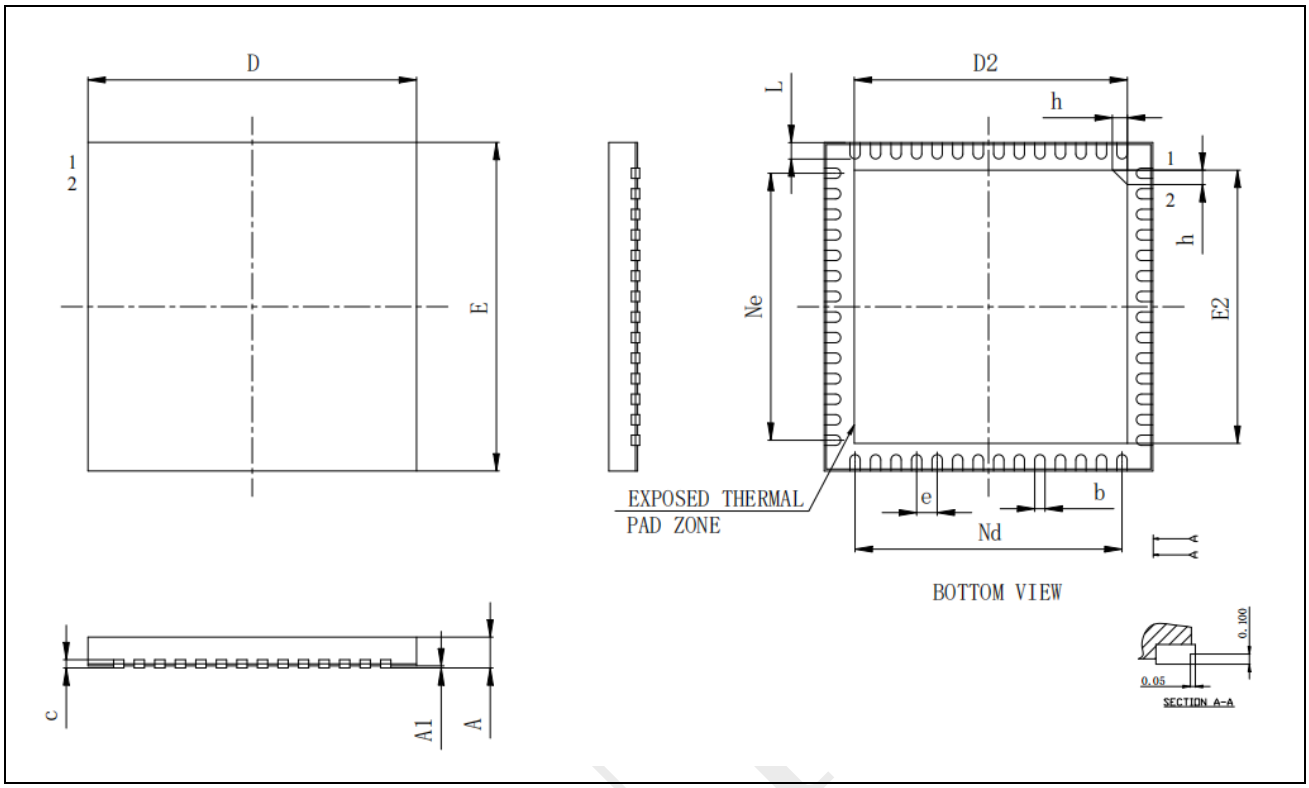


[1] Unit: mm

[2] Region A, B, C and D should be covered by solder paste, while region E has no special request.

6.2 QFN56 (Wettable Flank)

Figure 6-3: QFN56 - 56 pin, 8 x 8 mm wettable flank quad flat no-lead package outline



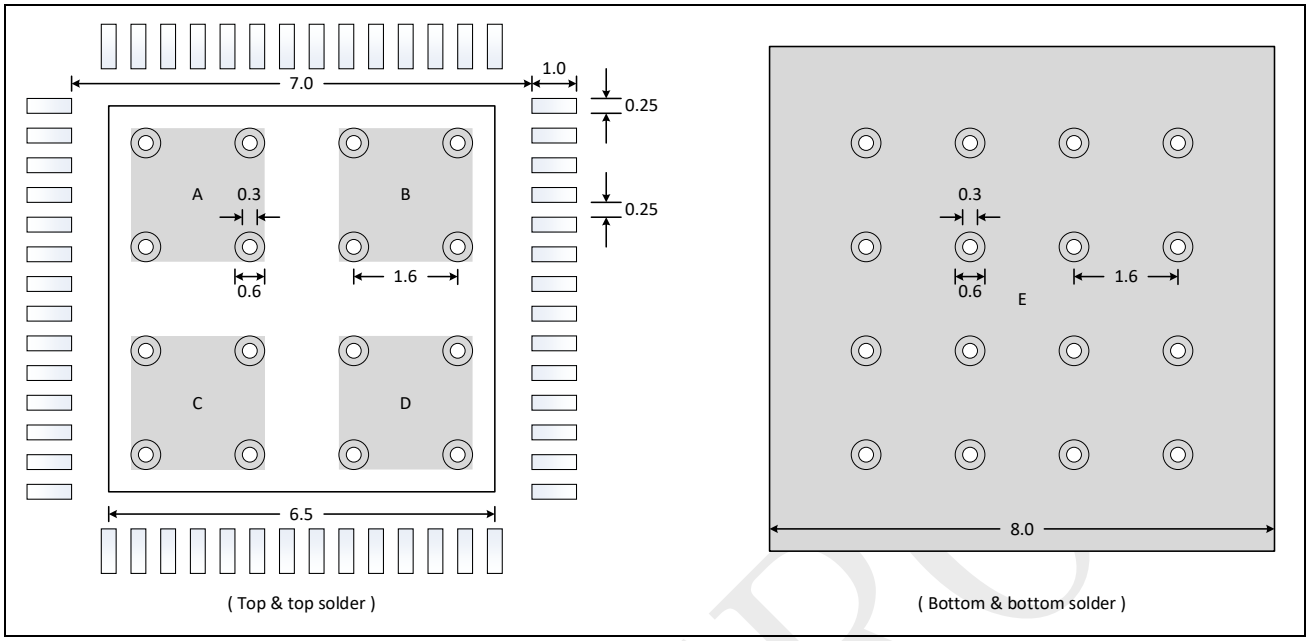
[1] Drawing is not to scale.

[2] The package mechanical data may be adjusted in future.

Table 6-2: QFN56 - 56 pin, 8 x 8 mm wettable flank quad flat no-lead package mechanical data

Symbol	Millimeter		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	6.55	6.65	6.75
e	0.50BSC		
Ne	6.50BSC		
Nd	6.50BSC		
E	7.90	8.00	8.10
E2	6.55	6.65	6.75
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 6-4: QFN56 - 56 pin, 8 x 8 mm wettable flank quad flat no-lead package recommended footprint



[1] Unit: mm

[2] Region A, B, C and D should be covered by solder paste, while region E has no special request.

7 Ordering information

Table 7-1: Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Pre-Driver	Package	Grade	SPQ[1]	Packing
SPD1179DPW48	128KB	32KB	100MHz	3 Phase	QFN48	Automotive AEC-Q100 Grade 1	4160	Tray
SPD1179ZDPW48	64KB	16KB	100MHz	3 Phase	QFN48	Automotive AEC-Q100 Grade 1	4160	Tray
SPD1179YDPW48	64KB	16KB	100MHz	2 Phase	QFN48	Automotive AEC-Q100 Grade 1	4160	Tray
SPD1179XDPW48	128KB	32KB	100MHz	2 Phase	QFN48	Automotive AEC-Q100 Grade 1	4160	Tray
SPD1179DPW56	128KB	32KB	100MHz	3 Phase	QFN56	Automotive AEC-Q100 Grade 1	3480	Tray
SPD1179YDPW56	64KB	16KB	100MHz	2 Phase	QFN56	Automotive AEC-Q100 Grade 1	3480	Tray
SPD1179XDPW56	128KB	32KB	100MHz	2 Phase	QFN56	Automotive AEC-Q100 Grade 1	3480	Tray
SPD1176APW48	128KB	32KB	100MHz	3 Phase	QFN48	Industrial	4160	Tray
SPD1176ZAPW48	64KB	16KB	100MHz	3 Phase	QFN48	Industrial	4160	Tray
SPD1176APW56	128KB	32KB	100MHz	3 Phase	QFN56	Industrial	3480	Tray

[1] SPQ = Standard Pack Quantity.

7.1 Rule of ordering number

Figure 7-1: Rule of ordering number