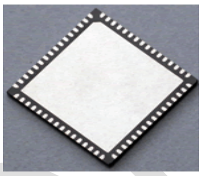
SPD1178 Datasheet

32-bit MCU
with 14-bit ADC, 3 PGA's Integrated double 3-phase Pre-Drivers and supply up to 60V

Features

- 32-bit ARM Cortex-M4 CPU Core with FPU
  - 200MHz maximum frequency
- Memories
  - Up to 128 KB embedded flash
  - 512 Bytes OTP flash
  - Up to 64 KB on-chip SRAM
- Pre-Driver Module
  - Two 3-Phase Pre-Drivers for dual BLDC motor control application with 60V max input voltage
  - Integrated bootstrap diodes
  - Integrated charge pump up to 100% duty cycle
  - Max 1A pull-up and 1.3A pull-down driving capability on each phase
  - Programmable output swing from 9V to 18V
  - Six V_{DS} monitors to current limit on each of the external high side FET's and short detection
- Clock, reset and supply management
  - Brown-out Detect (BOD) on each power rail
  - 3.3V power supply for MCU
  - Power-On Reset (POR)
  - 1 to 66 MHz external crystal oscillator
  - 32 MHz factory-trimmed oscillator
  - Typical 2.2MHz safety clock
  - PLL for CPU clock
- 14-bit A/D converters (up to 16 channels)
  - As low as 140 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sampler



QFN64 (8 x 8 mm)

  - Triple-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor
- Programmable gain amplifier (PGA)
  - Three integrated internal PGAs
  - Programmable Gains
    Single-ended: 1, 2, 4, 8, 12, 16, 24, 32
    Differential: 2, 4, 8, 16, 24, 32, 48, 64
  - Typical 600 ns settling time
- Analog comparator
  - Ten high-speed comparators
  - Output with digital deglitch filter
  - 4 DACs as reference
  - Optional DAC output buffer
  - Out of range voltage protection
  - Phase comparison
- PWM
  - Six enhanced PWM modules
  - 12 PWM outputs in total
  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 27 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin

  - Four 32-bit capture registers
  - Capture and PWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 6 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - SysTick timer 24-bit down-counter
- Communication interfaces
  - UART x 1 , SPI x 1, I^2C x 1, SIO x 1
  - SIO can be configure as CAN, UART, SPI, I2C
- Security Modules
  - CRC x 1, AES x 1, 64-bit unique ID
- Operating temperature
  - Junction temperature: -40 to +125 °C
  - Ambient temperature: -40 to +105 °C

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Revision history

Revision	Date	Author	Status	Changes
1	2019-04-01	-	Outdated	1. Initial release.
2	2019-04-11	-	Outdated	1. Modifies Table 3-1 for adding SIO pin definitions.
3	2020-05-20	-	Outdated	1. Modifies the description of power supply pin in Table 3-1. 2. Updates the maximum value of VBAT to 60V.
4	2019-08-15	-	Outdated	1. Updates package information in Table 7-1. 2. Modifies JTAG pin descriptions in Table 3-1.
5	2019-12-20	-	Outdated	1. Add Table 5-19. 2. Add Table 5-20.
6	2020-06-13	-	Outdated	1. Update Section 2.9 for boot mode description. 2. Update Section 2.14 and modify the maximum speed of SPI. 3. Update Section 2.18 for phase comparison. 4. Update Table 5-3. 5. Update Table 5-8. 6. Update Figure 5-2. 7. Add Table 5-9. 8. Add Table 5-10. 9. Add Table 5-11. 10. Add Table 5-12. 11. Update Table 5-13. 12. Add Table 5-22. 13. Add Table 5-23. 14. Add Table 8-1.
7	2020-07-04	-	Outdated	1. Update chip features. 2. Update Section 2.12 for UART features. 3. Update Table 5-14 and modify the value of R_{IN} parameter. 4. Update Table 5-25.
8	2020-07-31	-	Outdated	1. Add Figure 5-3. 2. Update Table 5-14. 3. Update Table 5-18.
9	2021-03-28	-	Outdated	1. Update Table 5-3. 2. Add characteristics of ambient temperature T_A. 3. Update Section 2.6. 4. Update Table 5-1. 5. Update Section 2.12 for UART features.

Revision	Date	Author	Status	Changes
				6. Update Table 5-14. 7. Update Figure 7-1. 8. Add Table 3-2. 9. Update comparator pin descriptions in Table 3-1. 10. Add Table 3-3. 11. Add note for Table 5-4. 12. Add note for Table 5-5. 13. Update Table 5-6. 14. Update Figure 3-1 and its notes.
10	2021-11-27	-	Outdated	1. Add Table 5-21. 2. Update Table 3-2. 3. Update Table 5-15. 4. Add Figure 5-4. 5. Add Figure 5-3. 6. Add Figure 5-6. 7. Add Figure 5-7. 8. Update Table 3-1, modify the description for debug pins. 9. Update deep-sleep current consumption value in Table 5-4.
11	2022-10-11	-	Outdated	1. Update Section 2.21. 2. Update Section 2.21, remove parameter I_{OZ}.
A/0	2022-05-22	Hengfang Huang	Outdated	1. Update Section 2.9 and Section 2.10. 2. Update Conditions of parameter R_{PU} and R_{PD} in Table 5-3. 3. Update Table 3-2. 4. Update Section 2.6.
A/1	2023-05-09	Lingzhi Chen	Outdated	1. Add VDDG maximum withstand voltage information.
C/0	2024-06-26	Jiali Zhou	Released	1. Modify document style.

Terms or abbreviations

Terms or abbreviations	Description
MCU	Microcontroller Unit
SWD	Serial Wire Debug
AHB	Advanced High Performance Bus
XIP	Execution In Place
PLL	Phase Locked Loop
BOD	Brownout Detector
PFD	Phase Frequency Detector
NVIC	Nested Vectored Interrupt Controller
UART	Universal Asynchronous Receiver-Transmitter
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
PGA	Programmable-Gain Amplifier
CRC	Cyclic Redundancy Check
AES	Advanced Encryption Standard

1 Device overview

The SPD1178 device from Spintrol is a highly integrated system-on-chip (SoC) microcontroller with dual 3-phase pre-drivers. The SPD1178 incorporates a 32-bit ARM Cortex-M4 high-performance processor with a software-programmable clock rate as high as 200 MHz, 64 KB SRAM, embedded flash with 128 KB, and an extensive range of enhanced I/Os and peripherals. The device offers a 14-bit ADC, three PGAs, six enhanced PWMs, three general purpose 32-bit timers, as well as standard and advanced communication interface: an UART, an I^{2}C and a SPI. These features make the SPD1178 ideal for motor control application.

The SPD1178 operates from a 2.97 to 3.63 V power supply for the MCU, and from 7V to 60V for the pre-driver. The temperature range is from -40 °C to +125 °C. The package type is 64-pin QFN.

Figure 1-1 shows the functional block diagram for the SPD1178. Figure 1-2 shows the clock tree information.

Figure 1-1: SPD1178 block diagram

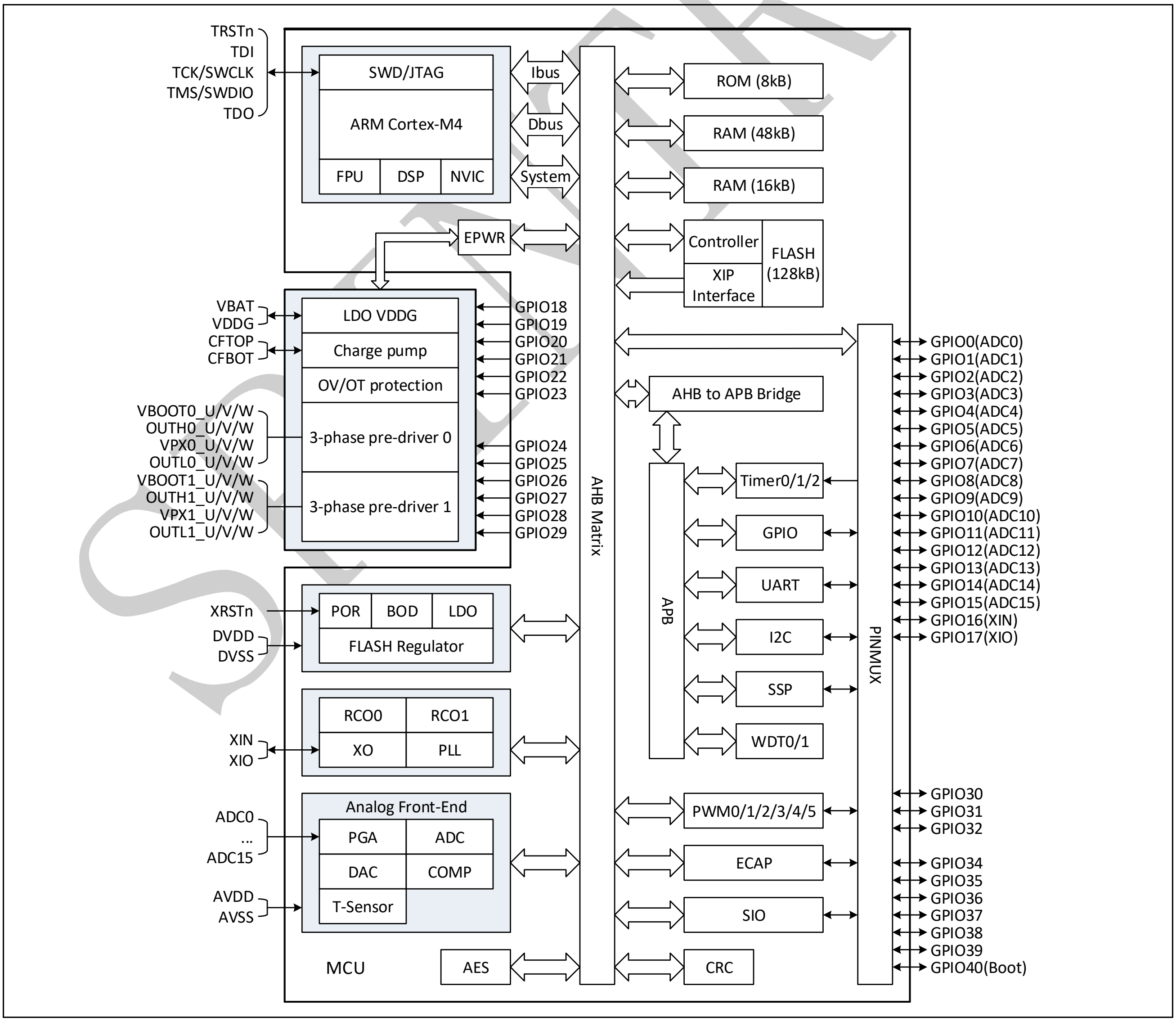
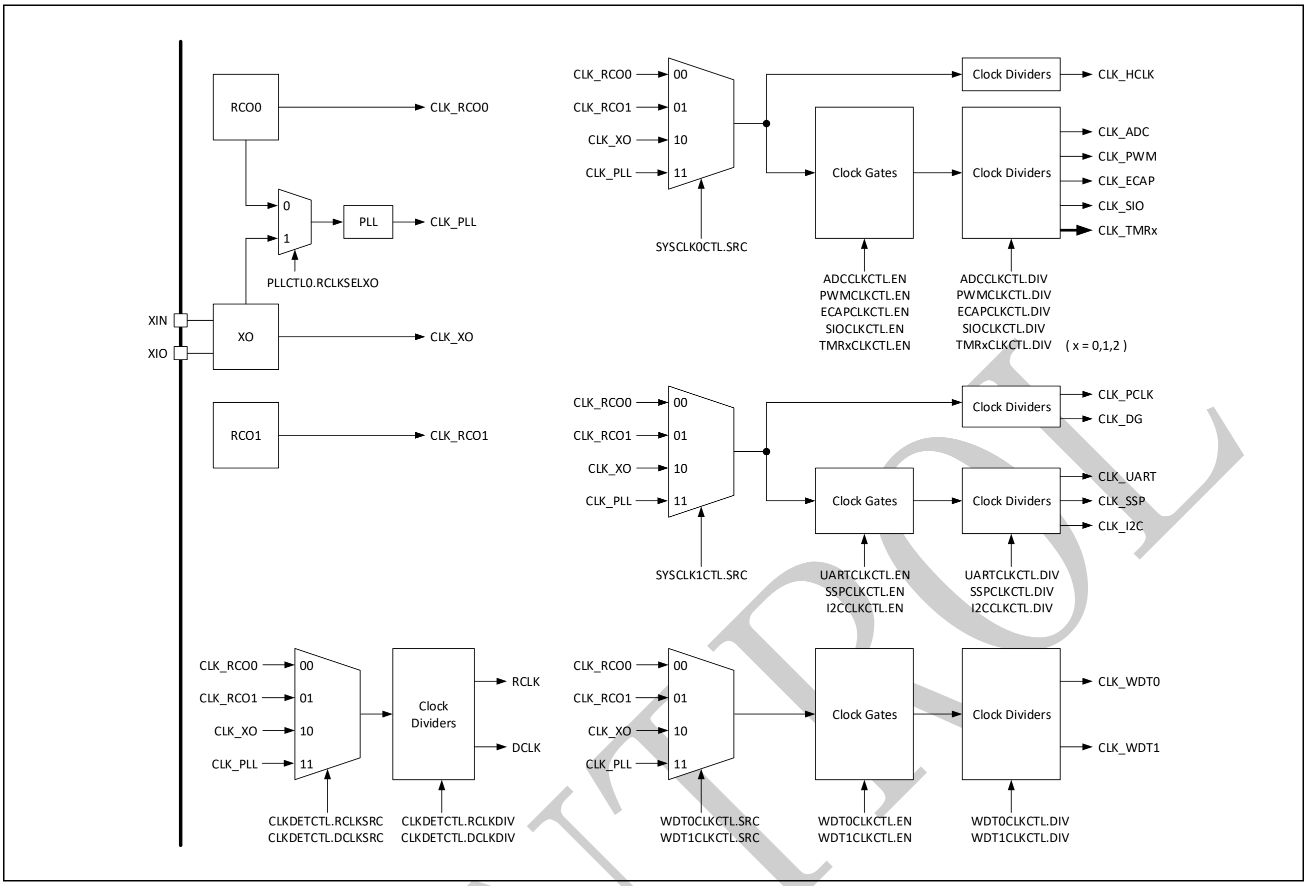


Figure 1-2: Clock tree



2 Feature descriptions

2.1 ARM Cortex-M4 core

The ARM Cortex-M4 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPD1178 integrates a full-feature ARM Cortex-M4 core with FPU that can run up to 200MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Embedded SRAM

The SPD1178 has implemented 64 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.3 Embedded Flash memory

Up to 128 KB of embedded Flash memory is available for storing programs and data.

2.4 Nested vectored interrupt controller (NVIC)

The SPD1178 embeds a nested vectored interrupt controller able to handle up to 51 mask-able interrupt channels (not including the 16 interrupt lines of Cortex-M4) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.5 External interrupt/event controller

The SPD1178 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.6 Power supply and Reset

The SPD1178 requires 3.3V power supply for the MCU, supply ramp-up rate less than or equal $1.5x10^4$V/s.

7V to 60V power supply for the pre-driver.

The SPD1178 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.7 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the 3.3V/1.2V domain power supply and compare it to the programmable pre-set value. An interrupt or reset can be generate when voltage of the power domain is higher or drops below the pre-set value. The interrupt service routine then generate a warning message and/or put the MCU into a safe state. The BOD is enabled by software.

2.8 Clocks

System clock selection is performed on startup. The internal 32 MHz RC oscillator is selected by default upon reset. An external 1 – 66 MHz oscillator can be selected by the user.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal RC oscillator or external clock as the input reference clock. The output frequency covers from 25MHz to 200MHz.

Several clock dividers allow the configuration of the AHB, APB and the peripherals frequency. The maximum allowed frequency is 200MHz for AHB and 50 MHz for APB. See Figure 1-2 for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 2.2MHz backup-safety oscillator makes the SPD1178 get rid of clock stuck.

2.9 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM. The boot pin and TRSTn pin are used to select one of the two boot options:

- Boot from embedded Flash (boot pin = 1, TRSTn pin = X): the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000
- ISP mode (boot pin = 0, TRSTn pin = 0): the boot loader reprograms the embedded Flash by using UART. During the process, the GPIO34 is configured as UART_TXD and the GPIO35 is configured as UART_RXD.

Note:	1. The boot pin should always keep high when chip normally running. The TRSTn pin is recommended to set as low. When TRSTn is high, the related debug interface pins (GPIO36 ~ GPIO39) must not be used as GPIO function.

2.10 General-purpose IOs (GPIOs)

The SPD1178 can be configured to support as many as 27 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter

2.11 Timers and watchdogs

The SPD1178 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPD1178 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. When the counter reaches zero, the timer can also generate an ADCSOC event or a PWMSYNC event if they are enabled. The clock of general-purpose timer can be selected from internal RC oscillators, external oscillator or PLL clock. Besides, each general-purpose timer can also capture external input as timer clock or enable signal.

Watchdogs

The SPD1178 implements two identical watchdogs. Each watchdog is based on a 32-bit down-counter, which can be clocked from internal RC oscillators, external oscillator or PLL clock. When the counter reaches the given time-out value, an interrupt or a reset can be generated. The watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

2.12 UART

The SPD1178 has an UART module that are functionally compatible with the 16550A and 16750 industry standards. It features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5 – 8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 12.5 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

2.13 I2C

The I^2C bus interface complies with the common I^2C protocol and can operate in standard mode (with data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s). It features:

- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.14 SPI

The SPI allows half/full-duplex, synchronous, serial communication with external devices. It features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- 50 Mbps maximum communication speed
- MSB-first data order
- Programmable clock polarity and phase
- Transmit and receive FIFOs

2.15 ADC

One 14-bit analog-to-digital convert is embedded into SPD1178 and has up to 16 external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has three independent built-in sample-and-hold (S/H). Each S/H has two input channels, which is suitable for differential sampling.

The events generated by the general-purpose timers and the PWM outputs can be internally connected to the ADC start trigger.

- 14-bit resolution
- 140 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Triple-sample and hold capability
- Simultaneous sampling and sequential sampling modes supported
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external
- Input open and short detection for safety

Please see Table 5-15 for ADC characteristics.

2.16 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

2.17 PGAs

Three flexible programmable gain amplifiers (PGAs) are embedded into SPD1178 and shares up to 16 channels. The temperature sensor and internal 1.2V power can be selected as a PGA input channels. These inputs are multiplexed. Each PGA outputs are connected to ADC input channel.

- Programmable gains

  Differential mode: 2, 4, 8, 16, 24, 32, 48, 64; Single-ended mode: 1, 2, 4, 8, 12, 16, 24, 32.

- Settling time: 400 ns to 800 ns

Please see Table 5-17 for PGA characteristics.

2.18 Analog comparators

The SPD1178 has ten high-speed comparators. Each comparator use the internal DAC as reference for monitoring PGA inputs or outputs. Two comparators are designed for each PGA: one is monitoring whether the voltage is too high, the other is monitoring whether the voltage is too low. The extra two pairs of comparators are reserved for additional applications. The comparator output is routed to the PWM Trip-Zone modules. Additionally, each comparator can implement the phase comparison for motor commutation. The detail channel selection can be referred to Technical Reference Manual.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter
- Phase comparison

Please see Table 5-18 and Table 5-19 for analog comparator and DAC characteristics.

2.19 PWMs

The SPD1178 integrates six PWM modules and supports 12 PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.20 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPD1178 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.21 Cyclic redundancy check (CRC)

The SPD1178 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation

− Five CRC standard polynomials supported

2.22 Advanced encryption standard (AES) engine

The AES engine provides fast hardware encryption and decryption services. The main features are as follows:

− Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO, and Bypass

− Supports 128-, 192-, and 256-bits key size

− Error indication for each block cipher mode

− Separate 4 x 32-bit input and output FIFOs

2.23 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port. The SWJ-DP interface enables either a serial wire debug or a JTAG probe to be connected to the target. The debug port can be disabled when enabling SPD1178 certain security feature.

2.24 SIO

SPD1178 has implemented an SIO module, which is based on a Spintrol patented technology. It has programmable capability that can convert the SIO module into pre-defined communication module. Currently the SIO can be used as UART, SPI, I2C and CAN once it is programmed through initialization. There will be more features added in short time.

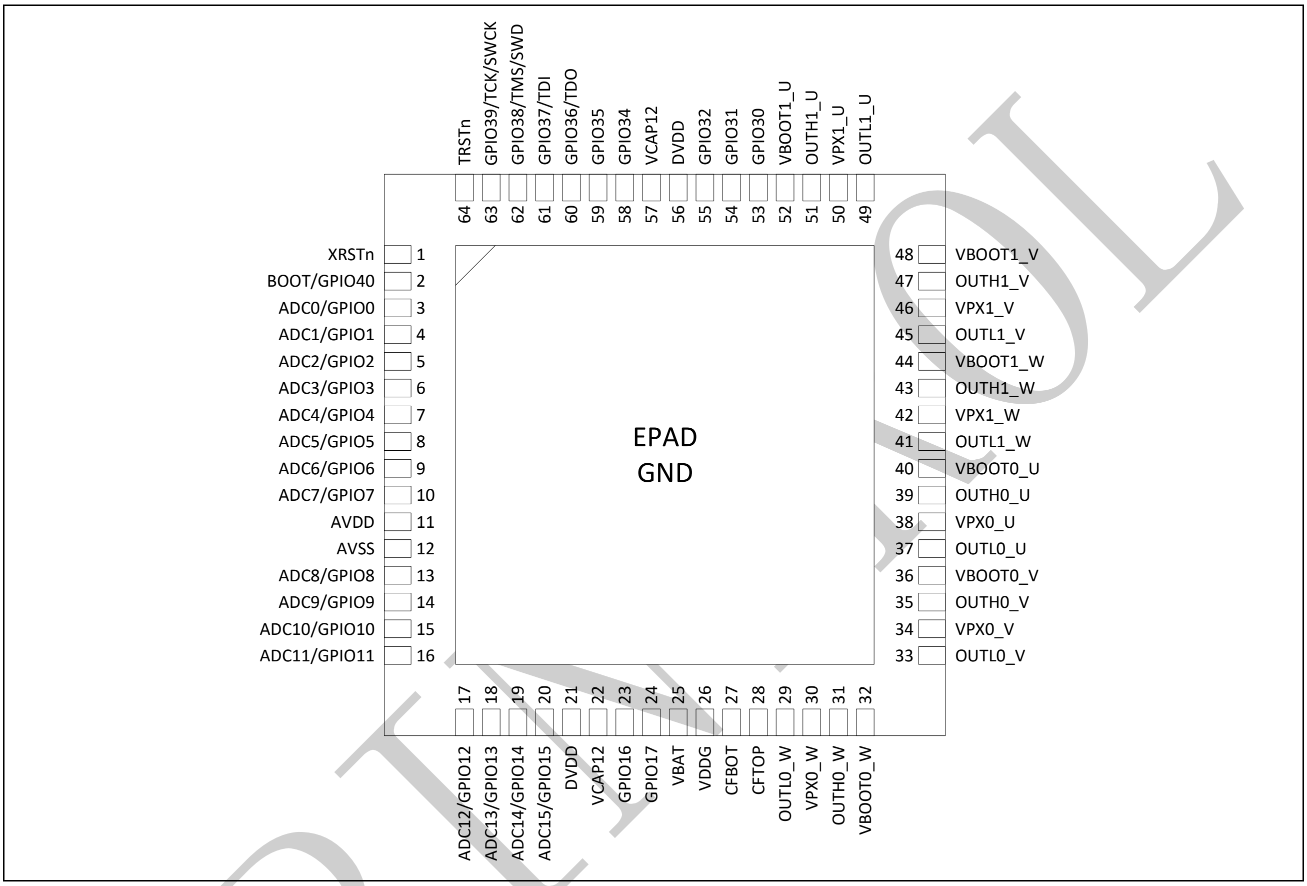
2.25 Pre-Driver system

Pre-driver system consists of two three-phase low- and high-side pre-drivers which drive low- and high-side external power NFET's or IGBT's. The voltage range of each low-side pre-driver is zero to V_{DDG}, which is typically 12V. The embedded charge pump guarantees 100% duty cycle, i.e. allows high-side of each phase to be on indefinitely without loss of charge on the high-side pre-driver stage. Additional features of pre-driver system include hardware-guaranteed input PWM non-overlap, monitoring external high-side power FET's drain-to-source voltage capability and local high-voltage area temperature monitoring.

3 Pinout and pin description

3.1 QFN64

Figure 3-1: SPD1178 QFN64 pin-out



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO36 ~ GPIO39 pins work as Debug interface and can't be configured as other functions.

Table 3-1: SPD1178 pin definitions

Pin	Signal	Type(1)	Description
1	XRSTn	I	Device reset pin, reset the device when low
2	BOOT (GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	DCLK	O	Clock output from CLKDET module for monitoring

Pin	Signal	Type(1)	Description
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	EPWRTZ1O	O	Trip-zone signal 1 from ePower module for monitoring
	SIO0_0	I/O	SIO0 input/output 0
3	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
4	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
5	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
6	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
7	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
8	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
9	GPIO6	I/O	General-purpose input/output 6
	ADC6	AI	ADC channel 6 input
10	GPIO7	I/O	General-purpose input/output 7
	ADC7	AI	ADC channel 7 input
11	AVDD	S	Analog power, add 4.7uF and 0.1uF bypass ceramic cap to AVSS
12	AVSS	S	Analog ground
13	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output

Pin	Signal	Type(1)	Description
	PWMSOC	O	PWM SOC signal output for monitoring
14	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
	COMP3L	O	Comparator COMP3L result output
15	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
16	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO(2)	O	Trip-zone signal from ePower module for monitoring
17	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	I2C_SCL	I/O	I^2C clock
18	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	I2C_SDA	I/O	I^2C data
19	GPIO14	I/O	General-purpose input/outpu14
	ADC14	AI	ADC channel 14 input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
20	GPIO15	I/O	General-purpose input/output 5
	ADC15	AI	ADC channel 15 input
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data

Pin	Signal	Type[1]	Description
21	DVDD	S	Digital power, add 4.7uF and 0.1uF bypass ceramic cap to GND
22	VCAP12	S	1.2V power, add 2.2uF bypass ceramic cap to GND
23	GPIO16	I/O	General-purpose input/output 16
	XIN	AI	External oscillator input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWM2A	O	PWM2 output A
	PWM5A	O	PWM5 output A
	SIO0_12	I/O	SIO0 input/output 12
24	GPIO17	I/O	General-purpose input/output 17
	XIO	AI/O	External oscillator input/output
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWM2B	O	PWM2 output B
	PWM5B	O	PWM5 output B
	SIO0_13	I/O	SIO0 input/output 13
25	VBAT	S	Main Supply Voltage, 7V to 60V, add 2.2uF bypass ceramic cap to GND
26	VDDG	S	VDDG LDO Output, 9V ~ 18V Programmable, add 2.2uF bypass ceramic cap to GND
27	CFBOT	S	Charge Pump Flying Capacitor Bottom Plate Voltage
28	CFTOP	S	Charge Pump Flying Capacitor Top Plate Voltage
29	OUTL0_W	O	Motor0 W-Phase Low Side FET Gate Drive
30	VPX0_W	O	Motor0 W-Phase Power FET Switching Node
31	OUTH0_W	O	Motor0 W-Phase High Side FET Gate Drive
32	VBOOT0_W	O	Motor0 W-Phase Bootstrap Pin
33	OUTL0_V	O	Motor0 V-Phase Low Side FET Gate Drive
34	VPX0_V	O	Motor0 V-Phase Power FET Switching Node
35	OUTH0_V	O	Motor0 V-Phase High Side FET Gate Drive
36	VBOOT0_V	O	Motor0 V-Phase Bootstrap Pin
37	OUTL0_U	O	Motor0 U-Phase Low Side FET Gate Drive

Pin	Signal	Type(1)	Description
38	VPX0_U	O	Motor0 U-Phase Power FET Switching Node
39	OUTH0_U	O	Motor0 U-Phase High Side FET Gate Drive
40	VBOOT0_U	O	Motor0 U-Phase Bootstrap Pin
41	OUTL1_W	O	Motor1 W-Phase Low Side FET Gate Drive
42	VPX1_W	O	Motor1 W-Phase Power FET Switching Node
43	OUTH1_W	O	Motor1 W-Phase High Side FET Gate Drive
44	VBOOT1_W	O	Motor1 W-Phase Bootstrap Pin
45	OUTL1_V	O	Motor1 V-Phase Low Side FET Gate Drive
46	VPX1_V	O	Motor1 V-Phase Power FET Switching Node
47	OUTH1_V	O	Motor1 V-Phase High Side FET Gate Drive
48	VBOOT1_V	O	Motor1 V-Phase Bootstrap Pin
49	OUTL1_U	O	Motor1 U-Phase Low Side FET Gate Drive
50	VPX1_U	O	Motor1 U-Phase Power FET Switching Node
51	OUTH1_U	O	Motor1 U-Phase High Side FET Gate Drive
52	VBOOT1_U	O	Motor1 U-Phase Bootstrap Pin
53	GPIO30	I/O	General-purpose input/output 30
	SPI_SCLK	I/O	SPI clock input/output
	I2C_SCL	I/O	I^2C clock
	COMP3H	O	Comparator COMP3H result output
	PWM3A	O	PWM3 output A
	PWM0A	O	PWM0 output A
	SIO0_8	I/O	SIO0 input/output 8
54	GPIO31	I/O	General-purpose input/output 31
	SPI_SFRM	I/O	SPI frame signal
	I2C_SDA	I/O	I^2C data
	COMP3L	O	Comparator COMP3L result output
	PWM3B	O	PWM3 output B
	PWM0B	O	PWM0 output B
	SIO0_9	I/O	SIO0 input/output 9
55	GPIO32	I/O	General-purpose input/output 32
	SPI_MOSI	I/O	SPI master output, slave input

Pin	Signal	Type(1)	Description
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
	PWM4A	O	PWM4 output A
	EPWRTZ0O	O	Trip-zone signal 0 from ePower module for monitoring
	SIO0_10	I/O	SIO0 input/output 10
56	DVDD	S	Digital power, add 0.1uF bypass ceramic cap to GND
57	VCAP12	S	1.2V power, add 0.1uF bypass ceramic cap to GND
58	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	SIO0_12	I/O	SIO0 input/output 12
59	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	SIO0_13	I/O	SIO0 input/output 13
60	GPIO36	I/O	General-purpose input/output 36
	TDO	O	JTAG data output
	UART_RXD	I	UART receive data
	SPI_SCLK	I/O	SPI clock input/output
	PWM5A	O	PWM5 output A
	PWM1A	O	PWM1 output A
	I2C_SDA	I/O	I^2C data
	SIO0_14	I/O	SIO0 input/output 14
	Note: when TRSTn is HIGH, this pin always works as TDO and can't be configured as other functions.		

<table>
<tr><th>Pin</th><th>Signal</th><th>Type(1)</th><th>Description</th></tr>
<tr><td rowspan="9">61</td><td>GPIO37</td><td>I/O</td><td>General-purpose input/output 37</td></tr>
<tr><td>TDI</td><td>I</td><td>JTAG data input</td></tr>
<tr><td>UART_TXD</td><td>O</td><td>UART transmit data</td></tr>
<tr><td>SPI_SFRM</td><td>I/O</td><td>SPI frame signal</td></tr>
<tr><td>PWM5B</td><td>O</td><td>PWM5 output B</td></tr>
<tr><td>PWM1B</td><td>O</td><td>PWM1 output B</td></tr>
<tr><td>I2C_SCL</td><td>I/O</td><td>I^2C clock</td></tr>
<tr><td>SIO0_15</td><td>I/O</td><td>SIO0 input/output 15</td></tr>
<tr><td colspan="3">Note: when TRSTn is HIGH, this pin always works as TDI and can't be configured as other functions.</td></tr>
<tr><td rowspan="8">62</td><td>GPIO38</td><td>I/O</td><td>General-purpose input/output 38</td></tr>
<tr><td>TMS/SWD</td><td>I/O</td><td>JTAG mode select or SWD data</td></tr>
<tr><td>I2C_SDA</td><td>I/O</td><td>I^2C data</td></tr>
<tr><td>SPI_MOSI</td><td>I/O</td><td>SPI master output, slave input</td></tr>
<tr><td>SPI_MISO</td><td>I/O</td><td>SPI master input, slave output</td></tr>
<tr><td>PWM2A</td><td>O</td><td>PWM2 output A</td></tr>
<tr><td>SIO0_16</td><td>I/O</td><td>SIO0 input/output 16</td></tr>
<tr><td colspan="3">Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.</td></tr>
<tr><td rowspan="8">63</td><td>GPIO39</td><td>I/O</td><td>General-purpose input/output 39</td></tr>
<tr><td>TCK/SWCK</td><td>I</td><td>JTAG clock or SWD clock</td></tr>
<tr><td>I2C_SCL</td><td>I/O</td><td>I^2C clock</td></tr>
<tr><td>SPI_MISO</td><td>I/O</td><td>SPI master input, slave output</td></tr>
<tr><td>SPI_MOSI</td><td>I/O</td><td>SPI master output, slave input</td></tr>
<tr><td>PWM2B</td><td>O</td><td>PWM2 output B</td></tr>
<tr><td>SIO0_17</td><td>I/O</td><td>SIO0 input/output 17</td></tr>
<tr><td colspan="3">Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.</td></tr>
<tr><td>64</td><td>TRSTn</td><td>I</td><td>JTAG reset pin, reset the JTAG when low</td></tr>
</table>

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] EPWRTZO signal is logic OR of EPWRTZ0O signal and EPWRTZ1O signal.

[3] All GPIO pins can be configured as ECAP input.

[4] All GPIO pins (except GPIO36 and GPIO37) can be configured as ECAP output.

3.2 PGA input channel selection

For the three on-MCU PGA's, each PGA has two 1-of-8 multiplexers (MUX) for input channel selection, one is for positive input (PGAx_P, x = 0,1,2) and the other is for negative input (PGAx_N, x = 0,1,2). The input channel selection table is shown below.

Table 3-2: PGA input channel selection

MUX Value	PGA0_P	PGA0_N	PGA1_P	PGA1_N	PGA2_P	PGA2_N
7	ADC4	ADC3	ADC9	ADC1	ADC14	ADC15
6	ADC10	ADC5	ADC10	ADC11	ADC12	ADC13
5	ADC8	ADC9	ADC8	ADC10	ADC8	ADC11
4	ADC6	ADC7	ADC2	ADC3	ADC4	ADC5
3	ADC0	ADC1	ADC0	ADC2	ADC0	ADC3
2	DAC2	DAC3	ATEST	VDD12	TSEN1(1)	TSEN0(1)
1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
0	GND	GND	GND	GND	GND	GND

[1] TSEN0 is output 0 of T-Sensor and TSEN1 is output 1 of T-Sensor.

3.3 GPIO pin function and state after reset

Table 3-3: GPIO pin function and state after reset

Pin Name	Default Function	Default State
GPIO0	ADC0	Floating
GPIO1	ADC1	Floating
GPIO2	ADC2	Floating
GPIO3	ADC3	Floating
GPIO4	ADC4	Floating
GPIO5	ADC5	Floating
GPIO6	ADC6	Floating
GPIO7	ADC7	Floating
GPIO8	ADC8	Floating
GPIO9	ADC9	Floating
GPIO10	ADC10	Floating
GPIO11	ADC11	Floating
GPIO12	ADC12	Floating
GPIO13	ADC13	Floating
GPIO14	ADC14	Floating
GPIO15	ADC15	Floating
GPIO16	GPIO16	Floating
GPIO17	GPIO17	Floating
GPIO18	GPIO18	Floating
GPIO19	GPIO19	Floating
GPIO20	GPIO20	Floating
GPIO21	GPIO21	Floating
GPIO22	GPIO22	Floating
GPIO23	GPIO23	Floating
GPIO24	GPIO24	Floating
GPIO25	GPIO25	Floating
GPIO26	GPIO26	Floating
GPIO27	GPIO27	Floating

Pin Name	Default Function	Default State
GPIO28	GPIO28	Floating
GPIO29	GPIO29	Floating
GPIO30	GPIO30	Floating
GPIO31	GPIO31	Floating
GPIO32	GPIO32	Floating
~~GPIO33~~	~~GPIO33~~	Floating
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up
GPIO36	GPIO36	Floating
GPIO37	GPIO37	Floating
GPIO38	GPIO38	Floating
GPIO39	GPIO39	Floating
GPIO40	GPIO40/BOOT	Pull up

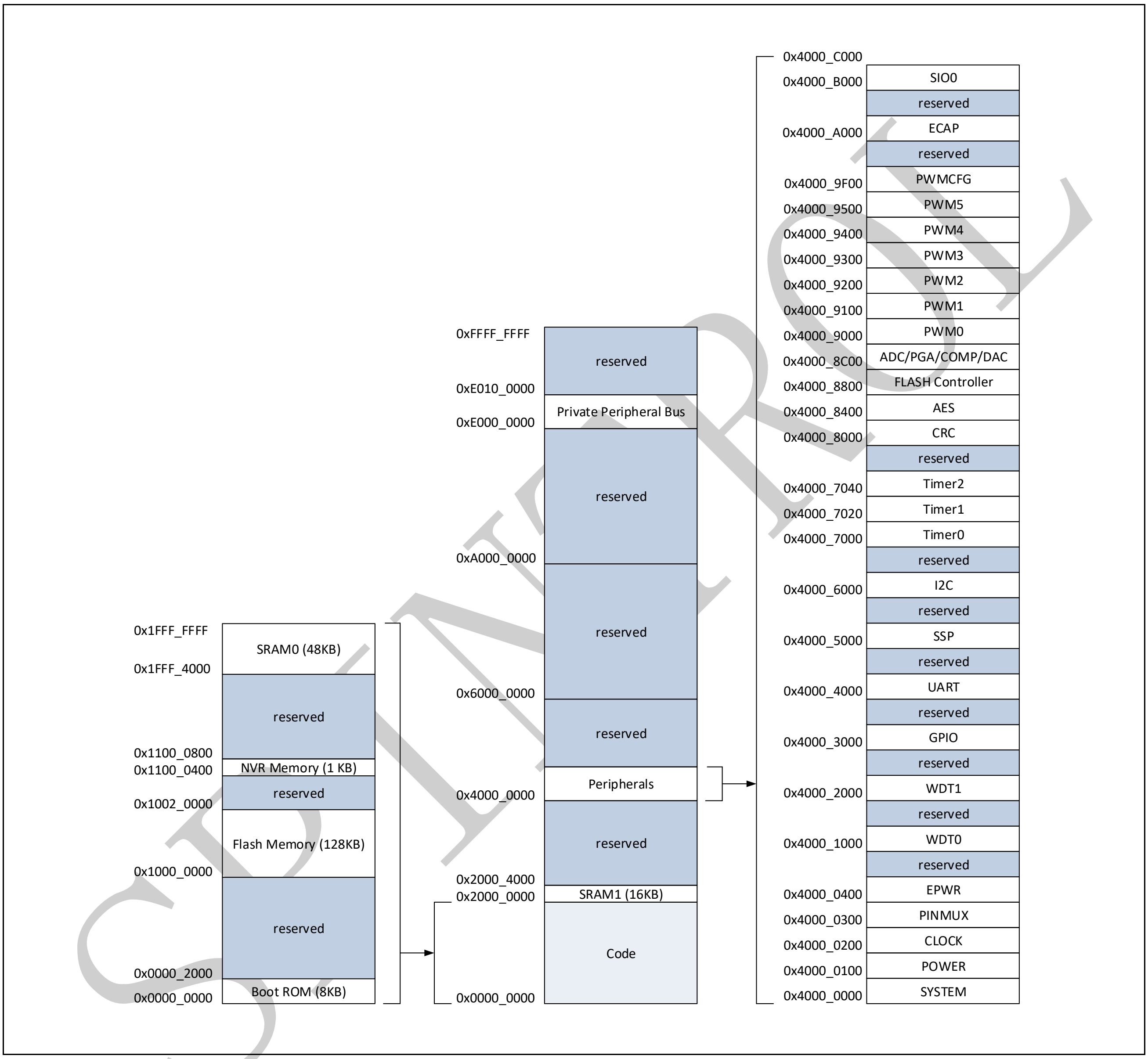
[1] In SPD1178, GPIO18~ GPIO29 are internally connected to the high voltage module, and not bonded out to the external pin.

[2] In SPD1178, the GPIOs with strikeout are not bonded out to the external pin.

4 Memory mapping

The memory map of SPD1178 is shown in Figure 4-1.

Figure 4-1: Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings (1)(2)

Symbol	Parameter	Min	Max	Unit
V_{BAT}	Pre-Driver supply voltage, with respect to V_{SS}	7	60	V
V_{BOOT}	Pre-Driver high-side power supply bootstrap voltage(4)	-	64	V
V_{DD}	Supply voltage, with respect to V_{SS}	-0.3	4.6	V
V_{DDG}	Pre-driver low-side voltage, with respect to V_{SS}	-0.3	18	V
V_{DDA}	Analog voltage, with respect to V_{SSA}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DD} = 3.3 V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature(3)	-40	+125	°C
T_A	Ambient temperature(3)	-40	+105	°C
T_{stg}	Storage temperature(3)	-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

[2] All voltage values are with respect to V_{SS}, unless otherwise noted.

[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

[4] Typically equal to VBAT+VDDG when high side of pre-driver turned on

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DD}	Supply voltage	-	2.97	3.3	3.63	V
V_{SS}	Supply ground	-	-	0	-	V
V_{DDA}	Analog supply voltage	-	2.97	3.3	3.63	V
V_{SSA}	Analog ground	-	-	0	-	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.8	V
I_{OH}	High-level output source current when $V_{OH} = V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL}	Low-level output sink current when $V_{OL} = V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
T_J	Junction temperature	-	-40	-	+125	°C
T_A	Ambient temperature	-	-40	-	+105	°C

5.3 I/O Electrical characteristics

Table 5-3: I/O Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	VDD-0.4	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	-	-	0.4	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V, V_{IH} = 0 V	-	-	2	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V, V_{IH} = V_{DD}	-	-	2	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	-	41	-	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DD}	-	42	-	kΩ

5.4 Power consumption summary

Typical current consumption

In operational mode, the SPD1178 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module) are enabled, except SIO module;
- All peripheral clocks are as fast as HCLK (frequency division is Zero), except SSP (Max 50 MHz) I2C (Max 50 MHz), PCLK (Max 50 MHz);
- All clock modules are enabled;

− Select PLL clock as system clock source.

In idle mode, the SPD1178 is placed under the following conditions:

− All I/O pins are in input mode and left unconnected;

− All peripherals(including analog module) are clocked off or disabled;

− Clock modules(PLL, RCO0 and XO) are disabled;

− Select RCO1 as system clock source.

In deep sleep mode, the SPD1178 is placed under the following conditions:

− All I/O pins are in input mode and left unconnected;

− All peripherals(including analog module) are clocked off or disabled;

− Clock modules(PLL, RCO1 and XO) are disabled;

− 1.2V LDO is shut down to 0V.

The typical current consumption of SPD1178 measured from V_{DD} is shown in Table 5-4 and Table 5-5. The operational current consumption over various HCLK frequency is shown in Figure 5-1.

Table 5-4: SPD1178 typical current consumption (Run in FLASH, Pre-Driver not included)

Mode	Conditions			Typ	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}		
Operational[1]	200 MHz[2]	50 MHz	200 MHz	67.937	mA
	175 MHz[2]	43.75 MHz	175 MHz	64.992	mA
	168 MHz[2]	42 MHz	168 MHz	64.006	mA
	150 MHz[2]	50 MHz	150 MHz	61.571	mA
	125 MHz[2]	41.67 MHz	125 MHz	58.123	mA
	100 MHz	50 MHz	100 MHz	54.551	mA
	75 MHz	37.5 MHz	75 MHz	50.904	mA
	50 MHz	50 MHz	50 MHz	47.389	mA
	32 MHz	32 MHz	32 MHz	44.353	mA
	25 MHz	25 MHz	25 MHz	43.309	mA
Idle	2.2 MHz	2.2 MHz	-	4.081	mA
Deep Sleep	-	-	-	10	uA

[1] Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

[2] SIO module clock frequency is f_{HCLK} / 2.

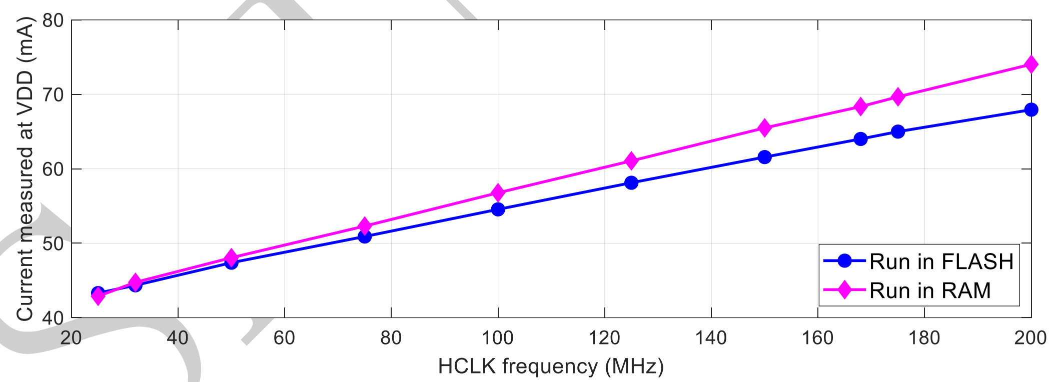
Table 5-5: SPD1178 typical current consumption (Run in RAM, Pre-Driver not included)

Mode	Conditions			Typ	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}		
Operational[1]	200 MHz[2]	50 MHz	200 MHz	74.035	mA
	175 MHz[2]	43.75 MHz	175 MHz	69.668	mA
	168 MHz[2]	42 MHz	168 MHz	68.354	mA
	150 MHz[2]	50 MHz	150 MHz	65.493	mA
	125 MHz[2]	41.67 MHz	125 MHz	61.061	mA
	100 MHz	50 MHz	100 MHz	56.777	mA
	75 MHz	37.5 MHz	75 MHz	52.305	mA
	50 MHz	50 MHz	50 MHz	48.059	mA
	32 MHz	32 MHz	32 MHz	44.752	mA
	25 MHz	25 MHz	25 MHz	42.883	mA
Idle	2.2 MHz	2.2 MHz	-	4.126	mA

[1] Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

[2] SIO module clock frequency is f_{HCLK} / 2.

Figure 5-1: Typical operational current versus frequency



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 5-6. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO0 and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
  - With all peripherals clocked disabled

➢ With only one peripheral enabled

Table 5-6: Peripheral current consumption

Peripherals[1]		Conditions	Typ[2]	Unit
BOD		Select RCO0 as system clock source; All other peripherals are in default settings; Close PLL, XO, RCO1 and RCO0 after disabling or enabling BOD module	0.1	mA
ADC	Analog[3]	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK; f_{HCLK} = 128 MHz, f_{PCLK} = 32 MHz, f_{PLL} = 128 MHz	16.52	mA
	Digital		0.31	mA
T-Sensor			0.16	mA
PGA[4]			4.10	mA
DAC			0.18	mA
Comparator			0.08	mA
UART		UART clock 200MHz, 256000 bps	0.416	mA
I2C		I2C clock 50MHz, 3.4Mbps	0.316	mA
SSP		SSP clock 50MHz, 50Mbps	0.361	mA
PWM		PWM clock 200MHz	1.471	mA
ECAP		ECAP clock 200MHz	0.329	mA
WDT		WDT clock 200MHz	0.245	mA
TMR		TMR clock 200MHz	0.385	mA
SIO		SIO clock 100MHz	6.63	mA
FLASH		HCLK clock 200MHz	0.772	mA
XO		HCLK is from 200MHz PLL, which takes RCO0 as input	0.616	mA
RCO		HCLK is from 200MHz PLL, which takes XO as input	0.313	mA
PLL		XO as HCLK source, f_{PLL} = 32 MHz	1.153	mA

[1] For peripherals with multiple instances, the current quoted is for single modules. For example, the 4.10 mA value quoted for PGA is for one PGA module. So the total 3 PGA module current is 12.30mA.

[2] Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

[3] ADC analog current contain ADC analog module, bandgap and ADC reference buffer.

[4] The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

Pre-Driver static current consumption

The Pre-Driver current consumption is measured additionally, shown as Table 5-7.

Table 5-7: Pre-Driver static current consumption

Peripherals	Conditions	Typ	Unit
Pre-Driver	EPWRCTL.EN is 0, VBAT input voltage is 12V.	3	uA
	EPWRCTL.EN is 0, VBAT input voltage is 60V.	19	uA
	EPWRCTL.EN is 1, Pre-Driver power off, VBAT input voltage bigger than 12V.	400	uA
	EPWRCTL.EN is 1, Pre-Driver power up, VBAT input voltage bigger than 12V, Output pin no loading and no toggling.	3300	uA

5.5 Internal 1.2V regulator characteristics

Table 5-8: Internal 1.2V regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply	-	2.97	3.3	3.63	V
VCAP12	Output voltage	Load current = 50mA	1.18	1.20	1.22	V
ΔVCAP12	Load regulation	VCAP12(50mA load) - VCAP12(200mA load)	-	-	30	mV

Table 5-9: Internal 1.2V regulator load regulation (TA = 25 °C)

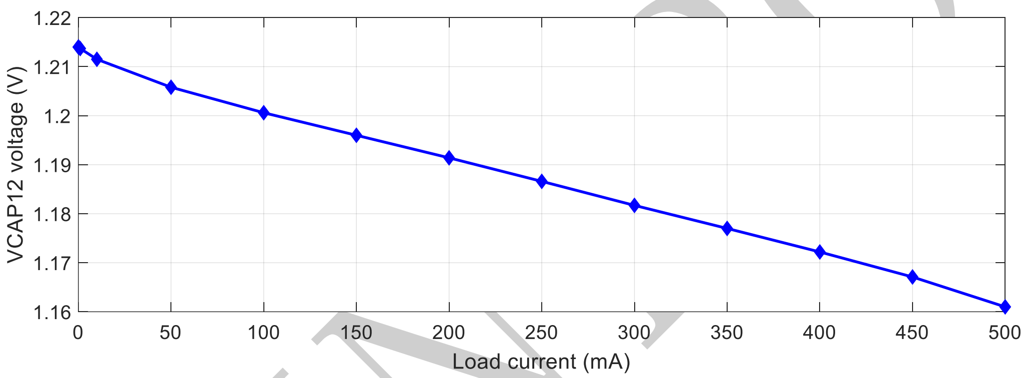
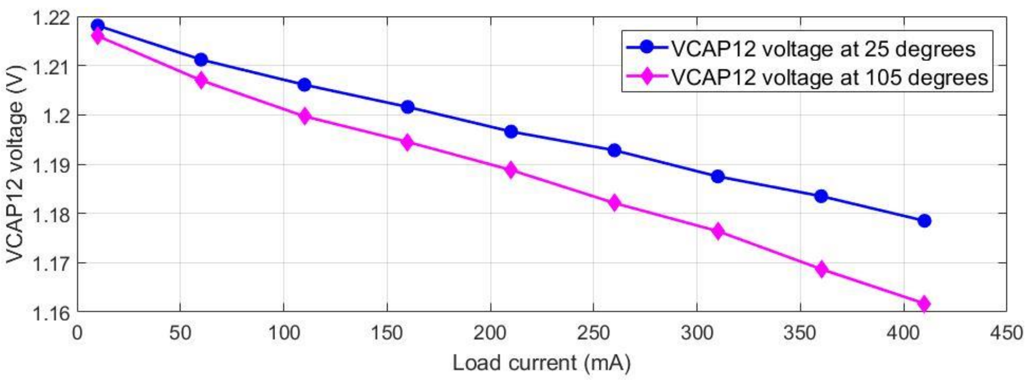


Table 5-10: Internal 1.2V regulator load regulation with different temperature



5.6 BOD characteristics

Table 5-11: BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{DD33H_Asset}	VDD33 too high assert threshold	-	-	3.42	-	V
$V_{DD33H\_Deasset}$	VDD33 too high de-assert threshold	-	-	3.31	-	V
V_{DD33L_Asset}	VDD33 too low assert threshold		-	2.58	-	V
$V_{DD33L\_Deasset}$	VDD33 too low de-assert threshold		-	2.65	-	V
V_{DD12H_Asset}	VDD12 too high assert threshold		-	1.33	-	V
$V_{DD12H\_Deasset}$	VDD12 too high de-assert threshold		-	1.31	-	V
V_{DD12L_Asset}	VDD12 too low assert threshold(1)		-	0.94	-	V
$V_{DD12L\_Deasset}$	VDD12 too low de-assert threshold(1)		-	0.97	-	V

[1] The characteristics of VDD12 too low 0 and VDD12 too low 1 are the same.

5.7 RCO characteristics

Table 5-12: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{RCO}	RCO frequency at room temperature	T_J = 25 °C	31.936	32.00	32.064	MHz
ACC_{RCO}	RCO frequency accuracy (RCO frequency variation versus temperature)	T_J = -40~125 °C	-1	-	1	%

5.8 PLL characteristics

Table 5-13: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{VCO}	VCO frequency	-	400	500	600	MHz
F_{pfd}	Phase-Frequency Detector (PFD) input frequency	-	4	-	8	MHz
t_{LOCK}	Locking time		-	-	15	us

5.9 XO characteristics

Table 5-14: XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{XO}	XO frequency	-	1	-	66	MHz

The negative resistance of the on-chip crystal oscillator at different temperature is shown in Figure 5-2 ~ Figure 5-5. The loading capacitor CL_eff is defined as equivalent capacitance seen by the on-chip crystal.

Figure 5-2: The negative resistance of the on-chip crystal oscillator at 50℃

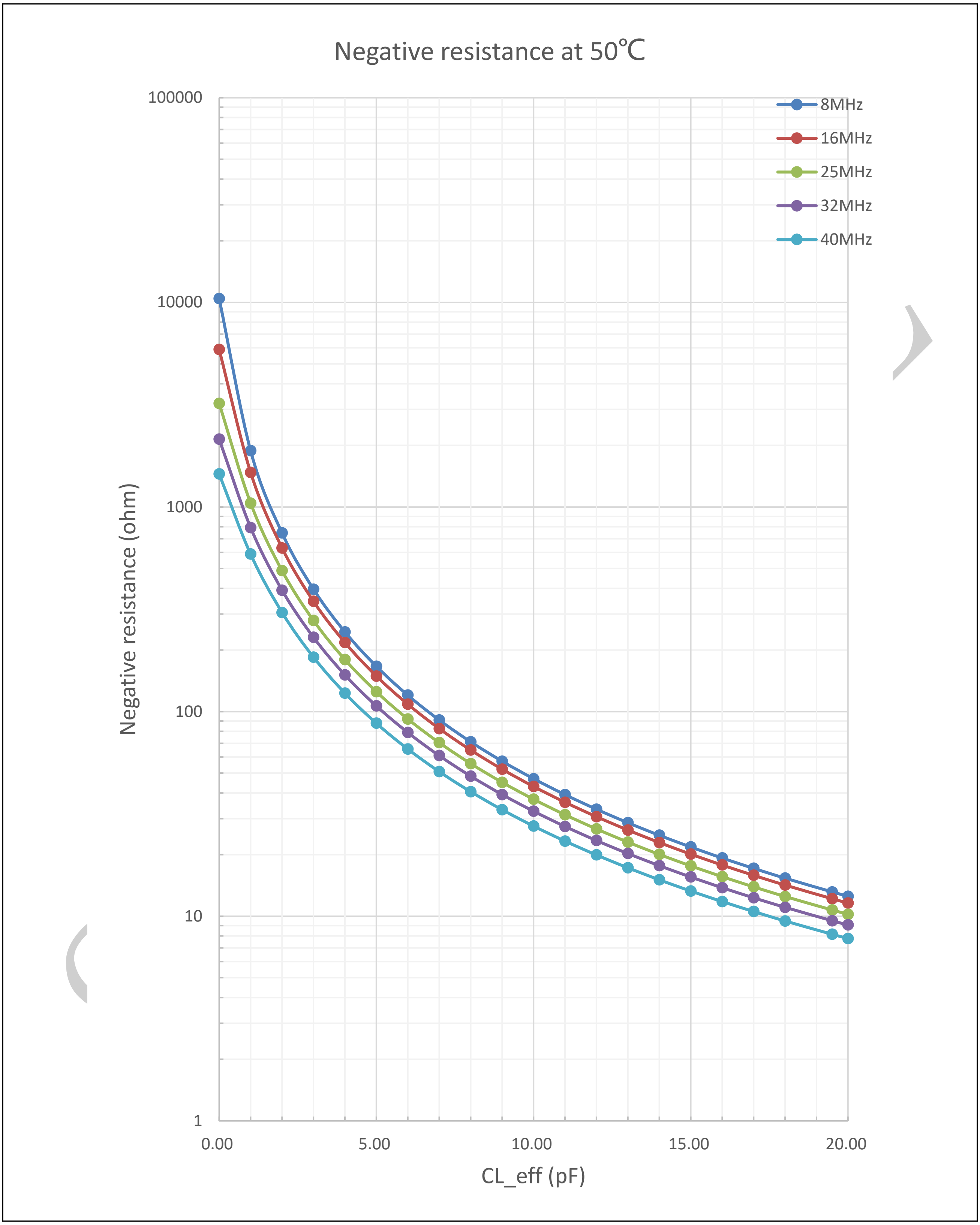


Figure 5-3: The negative resistance of the on-chip crystal oscillator at 85℃

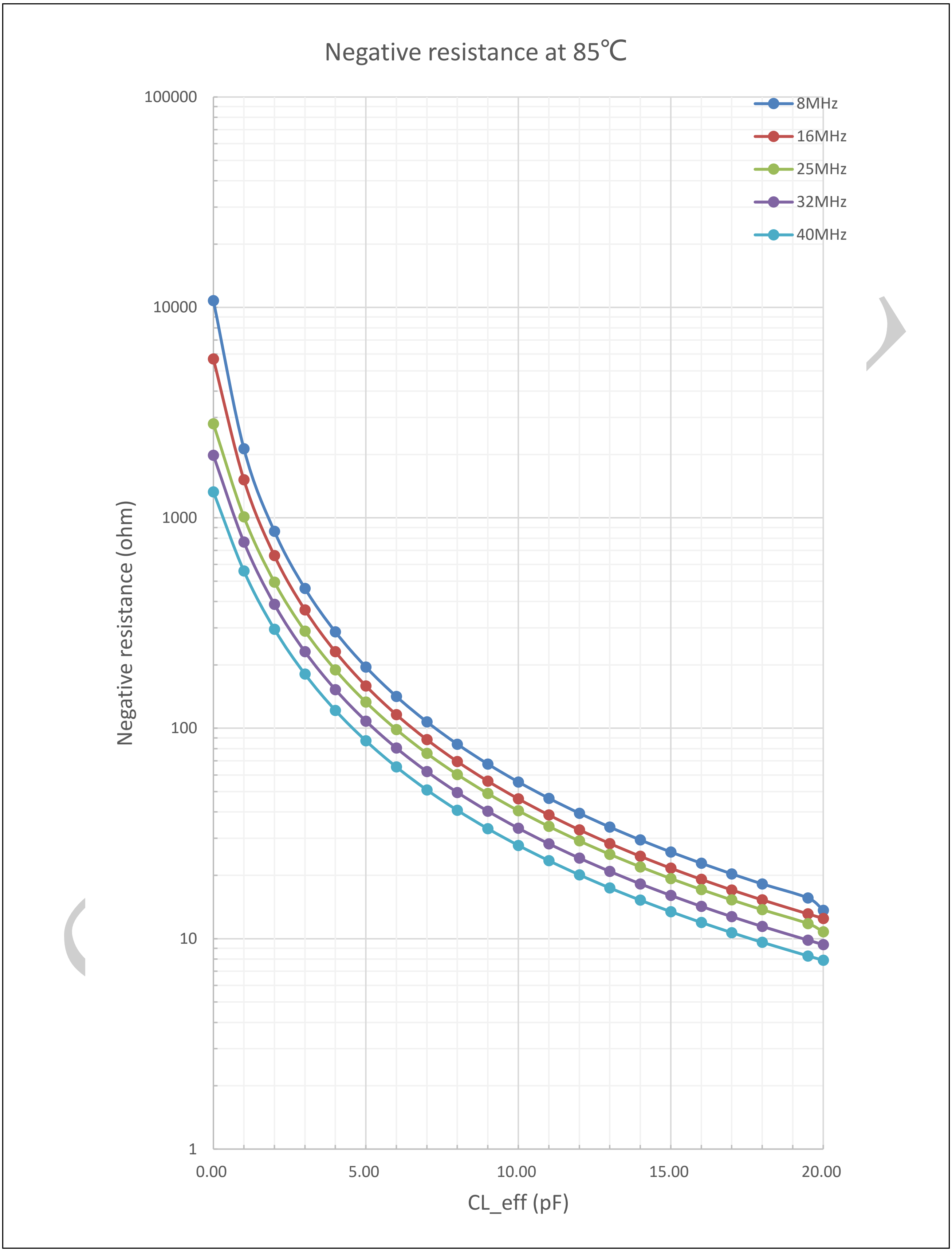


Figure 5-4: The negative resistance of the on-chip crystal oscillator at 100℃

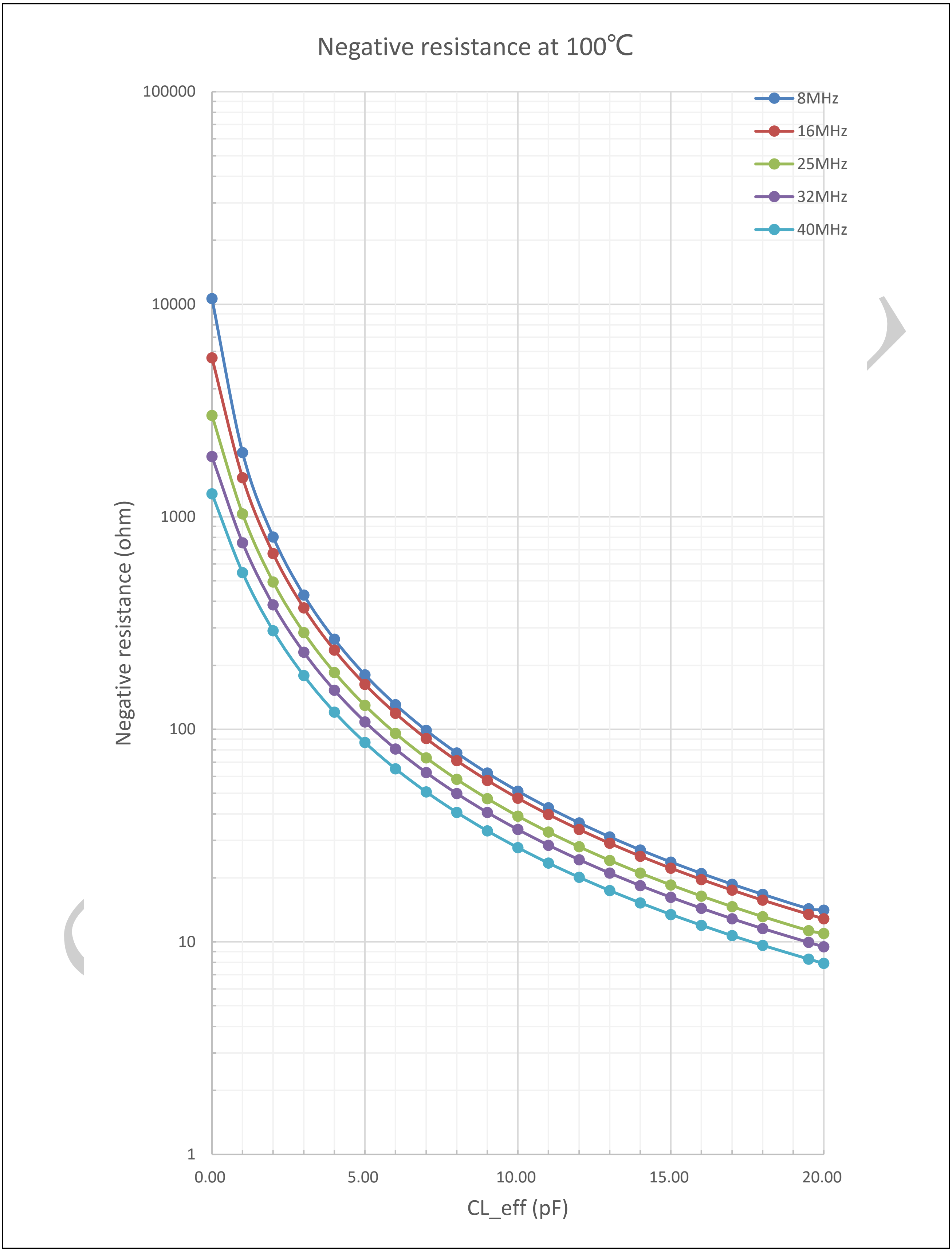
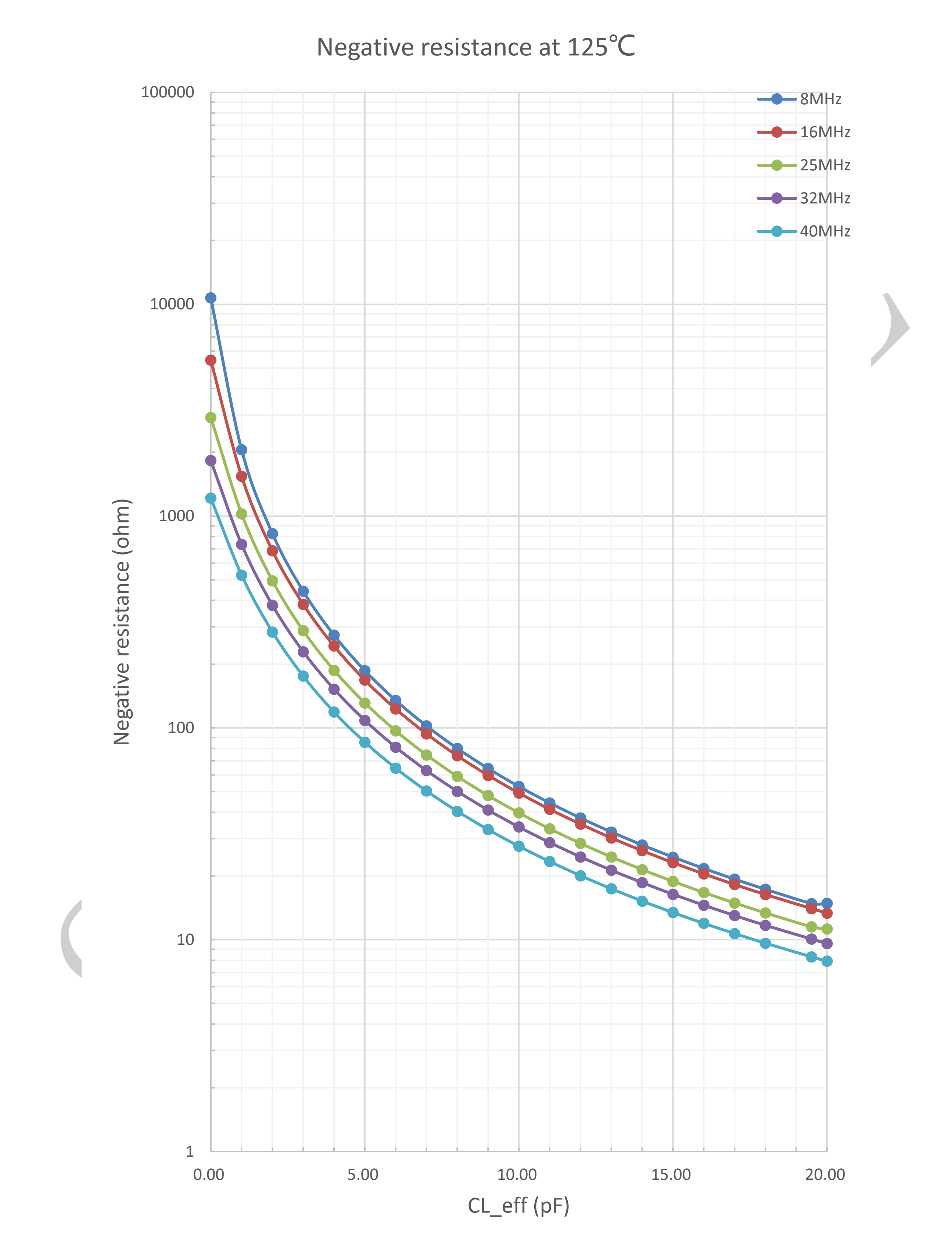


Figure 5-5: The negative resistance of the on-chip crystal oscillator at 125℃



5.10 14-bit ADC characteristics

Table 5-15: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	14	-	-	bit
F_S	Conversion speed[1]	-	-	-	4	MSPS
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{REF}	Reference voltage	-	1.194	1.2	1.206	V
I_{PAD}	Operational current	V_{DDA} = 3.3 V	-	17.1	21	mA
INL	Integral linearity error	-	-3.0	-	3.0	LSB
DNL	Differential linearity	-	-1.0	-	1.0	LSB
E_{OFF}	Offset error[2]	With calibration	-2	-	2	LSB
E_{GAIN}	Gain error[2]	With calibration	-4	-	4	LSB
E_{OFF2}	Channel to channel offset	-	-3	-	3	LSB
E_{GAIN2}	Channel to channel gain error	-	-5	-	5	LSB
T_{COEF}	ADC temperature coefficient with internal reference	-	-	26	-	ppm/°C
T_{PWRUP}	Power-up time	-	-	-	200	us
$ENOB_{DC}$	DC Noise Floor	-	-	12.0	-	bits
SNR	Signal-to-noise ratio	Fin = 100kHz, Amp = 0.94F_S, N = 8192	-	75.5	-	dB
THD	Total harmonic distortion		-	-85.0	-	dB
ENOB	Effective number of bits		-	12.2	-	bits
SFDR	Spurious free dynamic range		-	86.0	-	dB
T_{SLOPE}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	-	-	1.904[3]	-	°C/LSB
T_{OFFSET}	ADC output at 25 °C of the temperature sensor	-	-	162.138	-	LSB

[1] Sampling time = 110ns, conversion time = 140ns

[2] Offset and gain can be calibrated automatically by HW.

[3] Can be reduced to 0.24 °C/LSB by PGA.

5.11 PGA characteristics

Table 5-16: PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{OUT}	Output voltage range	-	0.3	-	V_{DDA}-0.3	V
R_{IN}	Input impedance	-	-	10	-	MΩ
G	Gain	Single-ended mode	1, 2, 4, 8, 12, 16, 24, 32			-
		Differential mode	2, 4, 8, 16, 24, 32, 48, 64			-
E_{GAIN}	Gain error	Differential Gain = 2	-0.5	-	0.5	%
		Differential Gain = 64	-3	-	3	%
V_{OS}	Offset	-	-5	-	5	mV
T_{OFFSET}	Offset temperature drift	-	-	5	-	uV/ °C
SR	Slew rate	Single mode and Loading is ADC sampling capacitor	-	20	-	V/us
		Differential mode and Loading is ADC sampling capacitor	-	40	-	V/us
GBW	Gain band width	Single gain = 1	-	40	-	MHz
		Single gain = 8	-	6.8	-	MHz
		Single gain = 32	-	1.7	-	MHz
		Differential gain = 2	-	20	-	MHz
		Differential gain = 16	-	3.4	-	MHz
		Differential gain = 64	-	0.8	-	MHz
t_{SETTLE}	Settle time	Differential gain = 2	-	170(1)	220	ns
		Differential gain = 16		400	600	ns
		Differential gain = 64	-	1600	2200	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	Differential gain = 2 Fin = 10kHz, Amp = 0.94F_S, N = 8192	-	74.0	-	dB
THD	Total harmonic distortion		-	-78.0	-	dB
ENOB	Effective number of bits		-	11.6	-	bit
SFDR	Spurious free dynamic range		-	82.0	-	dB
SNR	Signal-to-noise ratio	Differential gain = 64 Fin = 10kHz, Amp = 0.94F_S, N = 8192	-	58.0	-	dB
THD	Total harmonic distortion		-	-80.0	-	dB
ENOB	Effective number of bits		-	9.4	-	bit
SFDR	Spurious free dynamic range		-	63.0	-	dB
I	Current consumption	Only one PGA	-	4.16	5.20	mA

[1] Settle time is measured by step input, and differential output change from -2.7V to 2.7V (VDDA=3.3V), the time for output to be settled with 1LSB (446uV), guarantee by design.

5.12 Analog comparator characteristics

Table 5-17: Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage (Hysteresis voltage=0)	Common mode input voltage = 1.65V	-10	-	10	mV
V_{HYST}	Hysteresis voltage(12mV)	-	-	13	-	mV
	Hysteresis voltage(24mV)	-	-	26	-	mV
	Hysteresis voltage(36mV)	-	-	42	-	mV
t_D	Delay time – comparator response time to PWM shunt down (Asynchronous)	-	-	50	-	ns

5.13 Internal 10-bit DAC characteristics

Table 5-18: DAC characteristics

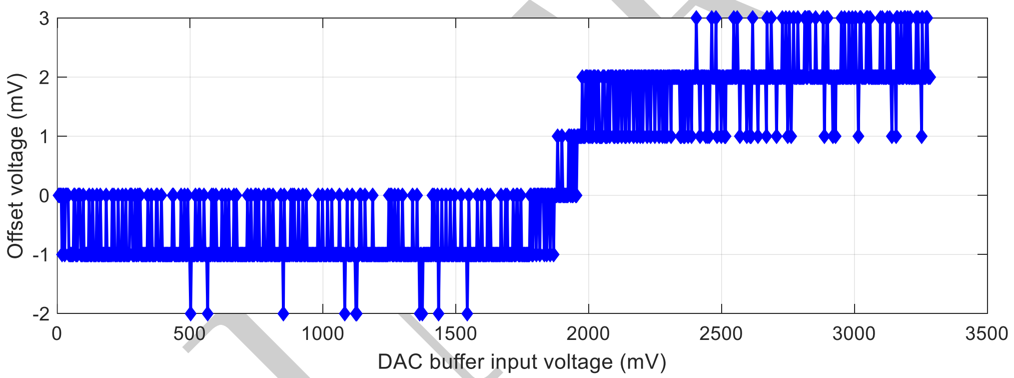
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N	resolution	Monotonic	10	-	-	bit
V_{FS}	Full scale value	-	0	-	V_{DDA}	V
DNL	Differential linearity	-	-0.5	-	0.5	LSB
INL	Integral linearity	-	-1	-	1	LSB
E_{OFF}	Offset error	-	-	5	-	mV
t_{SETTLE}	DAC settling time	Design guarantee	-	-	1	us

5.14 DAC buffer characteristics

Table 5-19: DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OUT}	Output voltage range	-	0.3	-	V_{DDA}-0.3	V
t_{SETTLE}	Settling time	Design guarantee	-	1	-	us
E_{OFF}	Offset error	-	-	3	-	mV
C_L	Capacitor load	-	-	-	50	pF
R_L	Resistor load	-	1	-		MΩ

Figure 5-6: DAC buffer offset over Input voltage



5.15 Flash memory characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 5-20: Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RD}	Read access time	-	40	-	ns
t_{PROG}	Word (32-bit) program time	-	8	10	us
t_{SE}	Sector erase time	-	0.8	4	ms
t_{CE}	Chip erase time	-	8	10	ms
N_{END}	Endurance (erase/program cycle)	T_J = 85 °C	100000	-	cycles
t_{RET}	Data retention duration	T_J = 85 °C	10	-	years

5.16 Electrical sensitivity characteristics

Table 5-21: ESD absolute maximum ratings

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Max</th><th>Unit</th></tr>
<tr><td>$V_{ESD(HBM)}$</td><td>Electrostatic discharge voltage (Human Body Model)</td><td colspan="2">Ambient temperature T_A = 25 °C</td><td>1000</td><td>V</td></tr>
<tr><td rowspan="2">$V_{ESD(CDM)}$</td><td rowspan="2">Electrostatic discharge voltage (Charge Device Model)</td><td rowspan="2">Ambient temperature T_A = 25 °C</td><td>-</td><td>500</td><td>V</td></tr>
<tr><td>Corner Pin</td><td>750</td><td>V</td></tr>
</table>

Table 5-22: Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 85 °C V_{DD} = 3.63V, VCAP12 = 1.32V	100	mA

5.17 Moisture sensitivity characteristics

Table 5-23: Moisture sensitivity characteristic

Symbol	Parameter	Conditions	Level	Unit
MSL	Moisture sensitivity level	-	Level 3	-

5.18 Thermal resistance characteristics

Table 5-24: Thermal resistance characteristics (QFN64 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	-	6.097	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	29.7742	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

5.19 SPI characteristics

Table 5-25: SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	-	-	-	50	MHz
$t_{SCLK(H)}$	SCLK clock high time	-	10	-	-	ns
$t_{SCLK(L)}$	SCLK clock low time	-	10	-	-	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(MO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(MI)}$	Data input setup time	-	6	-	-	ns
$t_{H(MI)}$	Data input hold time	-	2	-	-	ns
SPI slave mode						
$t_{SU(SFRM)}$	SFRM enable setup time	-	5.6	-	-	ns
$t_{H(SFRM)}$	SFRM enable hold time	-	1.5	-	-	ns
$t_{A(SO)}$	Data output access time	-	4	-	10	ns
$t_{DIS(SO)}$	Data output disable time	-	4	-	10	ns
$t_{V(SO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(SO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(SI)}$	Data input setup time	-	6	-	-	ns
$t_{H(SI)}$	Data input hold time	-	2	-	-	ns

5.20 Pre-Driver characteristics

Table 5-26: Pre-Driver characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
D_{MAX}	Maximum supported duty cycle	Charge pump will replenish bootstrap capacitor when high side is turned on	-	100	-	%
t_{DL}	Low-side propagation delay	1nF Capacitor as load	-	70	100	ns
t_{DH}	High-side propagation delay	1nF Capacitor as load	-	80	112	ns
Δt	High/Low side delay mismatch	-	-	-	4	ns
t_r	Rise time	1nF Capacitor as load	-	15	-	ns
t_f	Fall time	1nF Capacitor as load	-	10	-	ns
VPX_{MIN}	High side return ground Minimum	Min voltage where high side signal still propagate	-10	-	-	V
I_{Source_Max}	Pre-Driver Max sourcing capability	-	-	1	-	A
I_{Sink_Max}	Pre-Driver Max sinking capability	-	-	1.3	-	A

5.21 12V linear regulator characteristics

Table 5-27: 12V linear regulator characteristics

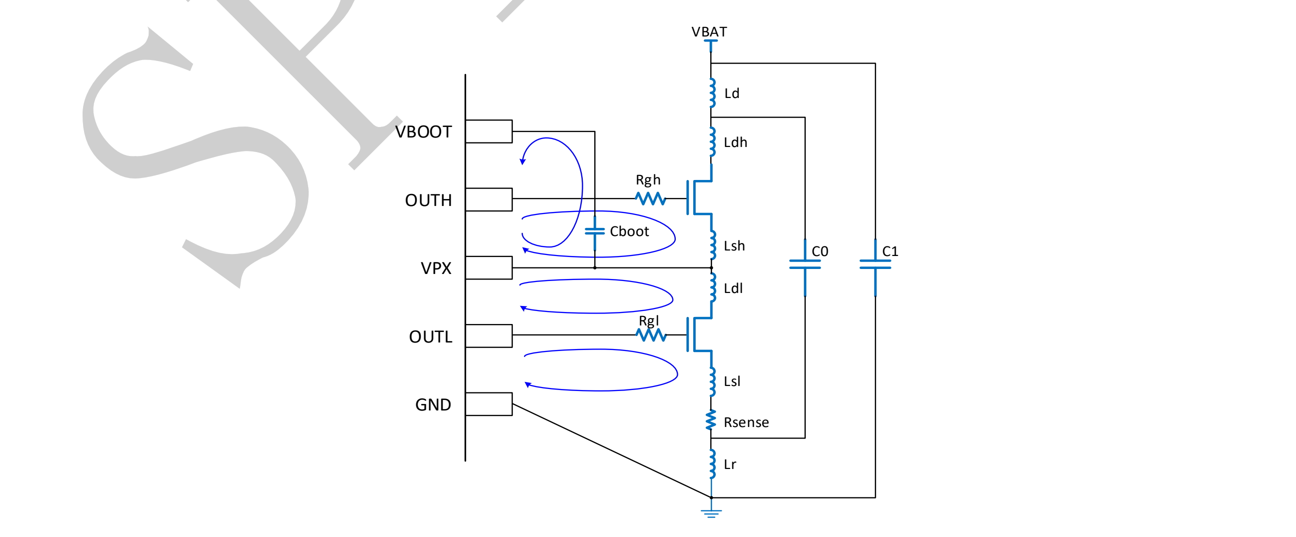
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDG	Pre-Driver low-side gate voltage	9V, 10V, 12V, 15V, 18V programmable	11.4	12	12.6	V
I_{VDDG_Limit}	LDO current limit	-	-	100	-	mA

[1] VDDG can't exceed VBAT. In general, VDDG value is minimum of programmable value or VBAT.

6 PCB layout guidance for Pre-Driver

- Co-locate power FET pairs with drain of low-side adjacent to source of high-side to minimize both Lsh and Ldl, and pairs placed close to each other to reduce routing distance and minimize Lr and Ld.
- Use thick, direct tracks between FET's with no loops or deviation.
- Minimize the areas of major current paths shown by arrows in the diagram of Figure 6-1 to avoid any loops.
- Avoid interconnect vias as they add significant inductance.
- In case of standing power FET's, reduce the effect of lead inductances by lowering package height above PCB.
- Connect the other end of C0 (shown in Figure 6-1) as close as possible to the drain of high-side FET, in order to provide the lowest-parasitic return path for current.
- Place pre-driver IC closer to power switches; route gate driver control signals OUTH and OUTL, and high- and low-side return grounds VPX and GND with straight as-short-as-possible traces.
- Connect bootstrap capacitor as close as possible to VPX and VBOOT pins.
- Connect low-ESR bypass capacitors from VBAT, VDDG and other power pins to ground, placing capacitors as close as possible to their respective pins, with the other end of each capacitor having a strong connection to board ground.
- Use power FET's with fast body diode turn-on times and as small as possible diode reverse charges.

Figure 6-1: Simplified Pre-Driver Board Schematic

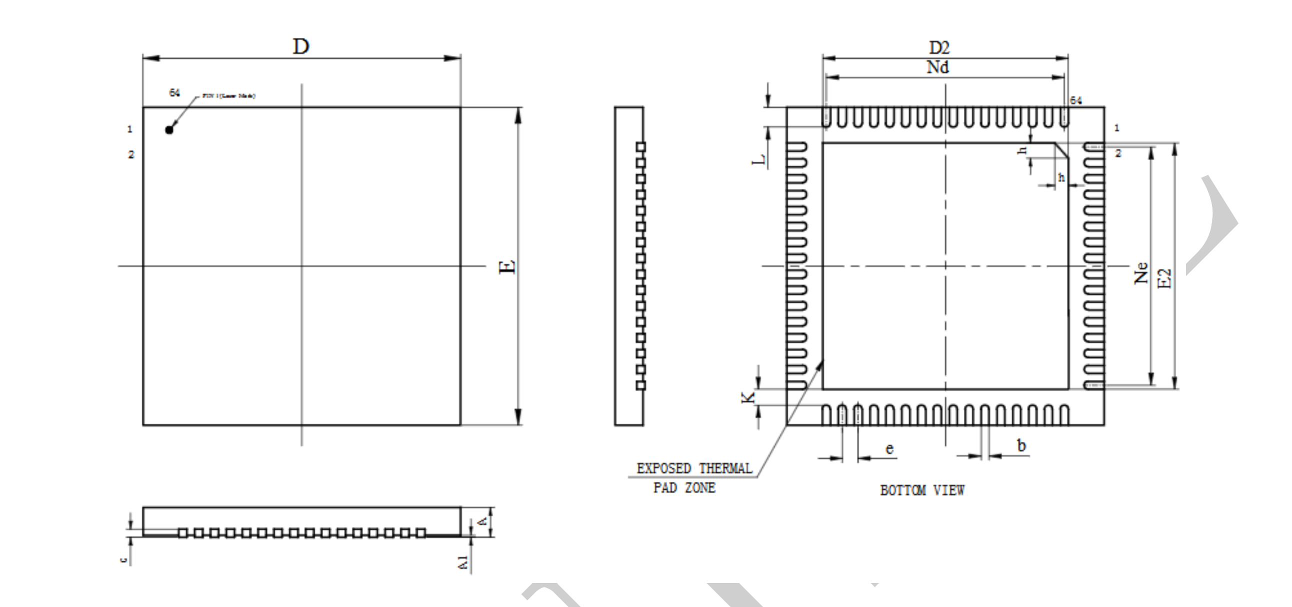


[1] This figure only shows the Pre-Driver one phase circuit diagram. And the Pre-Driver U-phase, V-phase and W-phase circuit diagrams are the same. Motor 0 and 1 signal routing concept are the same.

7 Package information

The package type of SPD1178 is 64-pin QFN. The detail information is as follows:

Figure 7-1: QFN64 – 64 pin, 8mm x 8 mm quad flat no-lead package outline



[1] Drawing is not to scale.

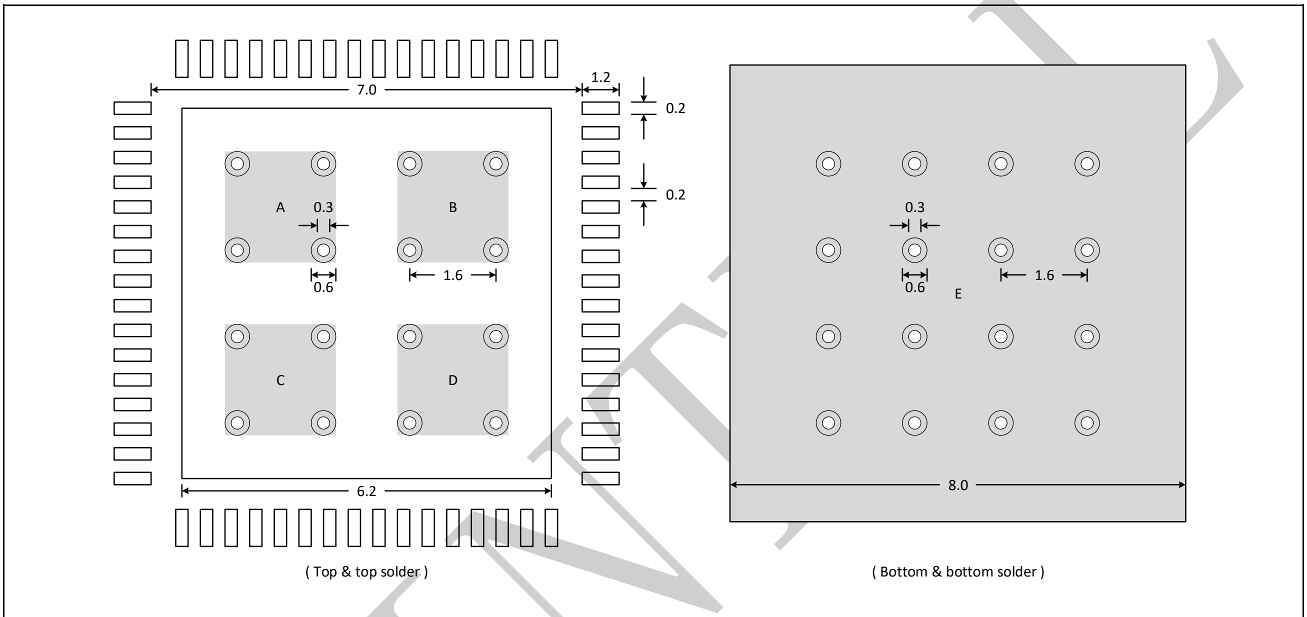
Table 7-1: QFN64 – 64 pin, 8mm x 8 mm quad flat no-lead package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	-	0.02	0.05	-	0.0008	0.0020
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
c	0.18	0.20	0.25	0.0071	0.0079	0.0098
D	7.90	8.00	8.10	0.3110	0.3150	0.3189
D2	6.10	6.20	6.30	0.2402	0.2441	0.2480
e	-	0.40	-	-	0.0157	-
Nd	-	6.00	-	-	0.2362	-
E	7.90	8.00	8.10	0.3110	0.3150	0.3189
E2	6.10	6.20	6.30	0.2402	0.2441	0.2480
Ne	-	6.00	-	-	0.2362	-
L	0.45	0.50	0.55	0.0177	0.0197	0.0217

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
K	0.20	-	-	0.0079	-	-
h	0.30	0.35	0.40	0.0118	0.0138	0.0157

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 7-2: QFN64 – 64 pin, 8mm x 8 mm quad flat no-lead package recommended footprint



[1] Dimensions are expressed in millimeters.

[2] The A, B, C, D areas on the top layer should brush solder paste, and E area on bottom layer can either brush solder paste or not.

8 Ordering information

Table 8-1: Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Package	Temperature Range	SPQ[1]	Packing
SPD1178API64	128KB	64KB	200MHz	QFN64	Industrial -40 °C to +125 °C	3480	Tray

[1] SPQ = Standard Pack Quantity.