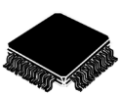
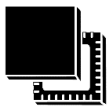
SPC1158 Datasheet

32-bit ARM Cortex-M4 based MCU with 11 channel PWMs, 16 channel 14-bit ADC, 3 PGAs with Comparators



LQFP48 (7 x 7 mm, 0.5mm pitch)
LQFP32 (7 x 7 mm, 0.8mm pitch)



QFN32 (5 x 5 mm)

Features

- ARM 32-bit Cortex-M4 CPU Core with FPU
  - 100 MHz maximum frequency
- Memories
  - Up to 128 KB embedded flash
  - 512 Bytes OTP flash
  - Up to 32 KB on-chip SRAM
- Clock, reset and supply management
  - Single 6.2~20 V power supply
  - Internal buck DC-DC with optional spread-spectrum capability to reduce EMI
  - POR, Brown-out detector (BOD)
  - 1-to-66 MHz external crystal oscillator
  - Internal 32MHz factory-trimmed oscillator
  - Internal 2.2MHz backup-safety oscillator
  - PLL for CPU clock
- 14-bit A/D converters (up to 16 channels)
  - As low as 140 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sample
  - Triple-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor
- Programmable gain amplifier (PGA)
  - Three integrated internal PGAs
  - Programmable Gains
    Single-ended: 1, 2, 4, 8, 12, 16, 24, 32
    Differential: 2, 4, 8, 16, 24, 32, 48, 64
  - Typical 600 ns settling time
- Analog comparator
  - Ten high-speed comparators
  - Output with digital deglitch filter
  - Four DACs as reference
  - Out of range voltage protection
  - Phase comparison
- PWM
  - Six enhanced PWM modules
  - 11 PWM outputs in total
  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 35 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and APWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 6 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - SysTick timer 24-bit down-counter
- Communication interfaces
  - UART x 1 , SPI x 1, I^2C x 1, SIO x 1
  - SIO can be configure as CAN, UART, SPI, I2C
- Security Modules

- CRC x 1, AES x 1, 64-bit unique ID

– Operating temperature
  - Junction temperature: -40 to +125 °C
  - Ambient temperature: -40 to +105 °C

Peripheral	SPC1158(H)APE48	SPC1158(H)APE32	SPC1158API32
Flash	64KB 128KB(H)	64KB 128KB(H)	64KB
OTP Flash	512Bytes	512Bytes	512Bytes
SRAM	32KB	32KB	32KB
GPIOs[1]	35	19	21
14-bit ADC Number of channels	1 16 channels	1 8 channels	1 9 channels
PGA	3	3	3
Analog comparators	10	10	10
DAC	4	4	4
PWM Number of channels	6 11 channels	6 8 channels	6 8 channels
ECAP	1	1	1
General-purpose timers	3	3	3
Watchdog timers	2	2	2
AES	1	1	1
CRC	1	1	1
UART	1	1	1
SPI	1	1	1
I2C	1	1	1
SIO	1	-	1
Maximum CPU frequency	100MHz	100MHz	100MHz

[1] Not including GPIO40 (BOOT) pin.

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Revision history

Revision	Date	Author	Status	Changes
1	2019-04-01	H. Huang	Outdated	1. Initial release.
2	2019-04-11	H. Huang	Outdated	1. Modifies Table 3-1 for adding SIO pin definitions. 2. Modifies Table 3-2 for adding SIO pin definitions.
3	2019-05-20	H. Huang	Outdated	1. Modifies description of power supply pin in Table 3-1. 2. Modifies description of power supply pin in Table 3-2.
4	2019-07-04	H. Huang	Outdated	1. Corrects QFP32 to QFN32.
5	2019-08-16	H. Huang	Outdated	1. Modifies JTAG pin descriptions in Table 3-1 and Table 3-2.
6	2020-12-20	H. Huang	Outdated	1. Add Table 5-19. 2. Add Table 5-20.
7	2020-06-13	H. Huang	Outdated	1. Update Section 2.9 for boot mode description. 2. Update Section 2.14 and modify the maximum speed of SPI. 3. Update Section 2.18 for phase comparison. 4. Update Table 5-3. 5. Update Table 5-8. 6. Update Table 5-9. 7. Add Table 5-9. 8. Add Table 5-10. 9. Add Table 5-11. 10. Add Table 5-12. 11. Update Table 5-13. 12. Add Table 5-22. 13. Add Table 5-24. 14. Add Table 5-25. 15. Add Table 8-1.
8	2020-07-04	H. Huang	Outdated	1. Update Section 2.12 for UART features. 2. Update Section 2.21 for CRC features. 3. Update Table 5-14 and modify the value of R_{IN} parameter.

Revision	Date	Author	Status	Changes
9	2020-07-20	H. Huang	Outdated	1. Add Figure 5-2. 2. Add Figure 5-5. 3. Update Table 5-14. 4. Update Table 5-18.
10	2021-03-16	H. Huang	Outdated	1. Update Table 5-3. 2. Add characteristics of ambient temperature T_A. 3. Update Section 2.12 for UART features. 4. Update Table 5-14. 5. Update Figure 7-4. 6. Add LQFP32 pinout and package information. 7. Add Table 3-4. 8. Update comparator pin descriptions in Table 3-1~ Table 3-3. 9. Add Table 3-5. 10. Update Figure 3-1 and its notes. 11. Update Figure 3-2 and its notes. 12. Update Figure 3-3 and its notes. 13. Update Table 5-19.
11	2021-11-26	H. Huang	Outdated	1. Add SPC1158 device features and peripheral counts. 2. Add Table 5-21. 3. Add Table 5-23. 4. Update Table 3-4. 5. Update SPC1158API32 information related SIO. 6. Update Table 5-2. 7. Update b, b1, c parameter values in Table 7-1. 8. Update Table 5-15. 9. Add Figure 5-6. 10. Add Figure 5-7. 11. Add Figure 5-8. 12. Add Figure 5-9. 13. Update Table 3-1, modify the description for debug pins.

Revision	Date	Author	Status	Changes
				14. Update Table 3-2, modify the description for debug pins. 15. Update Table 3-3, modify the description for debug pins.
12	2022-07-08	H. Huang	Outdated	1. Update Section 2.21. 2. Update Table 5-3, remove parameter I_{OZ}. 3. Add Chapter 6. 4. Update available PWM channel number. 5. Update maximum Flash memory size to 128KB. 6. Add information for SPC1158HAPE32. 7. Update Section 2.9 and Section 2.10. 8. Update Conditions of parameter R_{PU} and R_{PD} in Table 5-3. 9. Update Table 3-4.
13	2022-08-24	H. Huang	Outdated	1. Update Table 8-1, add SPC1158HAPE48.
A/0	2023-02-17	C.Hu	Outdated	1. Add clamping diode description in Table 5-3.
A/1	2023-03-06	L.Chen C.Hu	Outdated	1. Stress that DVDD should be connected on PCB board in section 3.1, 3.2,3.3. 2. Update SW_DCDC type in Section 3.1, 3.2, 3.3
C/0	2024-04-20	J.Zhou	Outdated	1. Update Section 2.12. 2. Modify document style.
C/1	2024-12-13	J.Zhou	Released	1. Update Table 5-1. 2. Add performance description for DAC waveform generation.

Terms or abbreviations

Terms or abbreviations	Description
MCU	Microcontroller Unit
SWD	Serial Wire Debug
AHB	Advanced High Performance Bus
XIP	Execution In Place
PLL	Phase Locked Loop
BOD	Brownout Detector
PFD	Phase Frequency Detector
NVIC	Nested Vectored Interrupt Controller
UART	Universal Asynchronous Receiver-Transmitter
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
PGA	Programmable-Gain Amplifier
CRC	Cyclic Redundancy Check
AES	Advanced Encryption Standard

1 Device overview

The SPC1158 device from Spintrol is a highly integrated system-on-chip (SoC) microcontroller with DC/DC module. The SPC1158 incorporates a 32-bit ARM Cortex-M4 high-performance processor with a software-programmable clock rate as high as 100 MHz, 32 KB SRAM, embedded flash with 128 KB, and an extensive range of enhanced I/Os and peripherals. The device offers a 14-bit ADC, three PGAs, six enhanced PWMs, three general purpose 32-bit timers, as well as standard and advanced communication interface: an UART, an I2C and a SPI. These features make the SPC1158 ideal for motor control application.

The SPC1158 operates with internal DC/DC, which takes input voltage from 6.2V to 20V, and generate 3.3V power supply. Alternative option to use external 3.3V supply is also supported. The temperature range is from -40 oC to +125 oC. The package type is 48-pin LQFP, 32-pin LQFP or 32-pin QFN.

Figure 1-1 shows the functional block diagram for the SPC1158. Figure 1-2 shows the clock tree information.

Figure 1-1: SPC1158 Block diagram

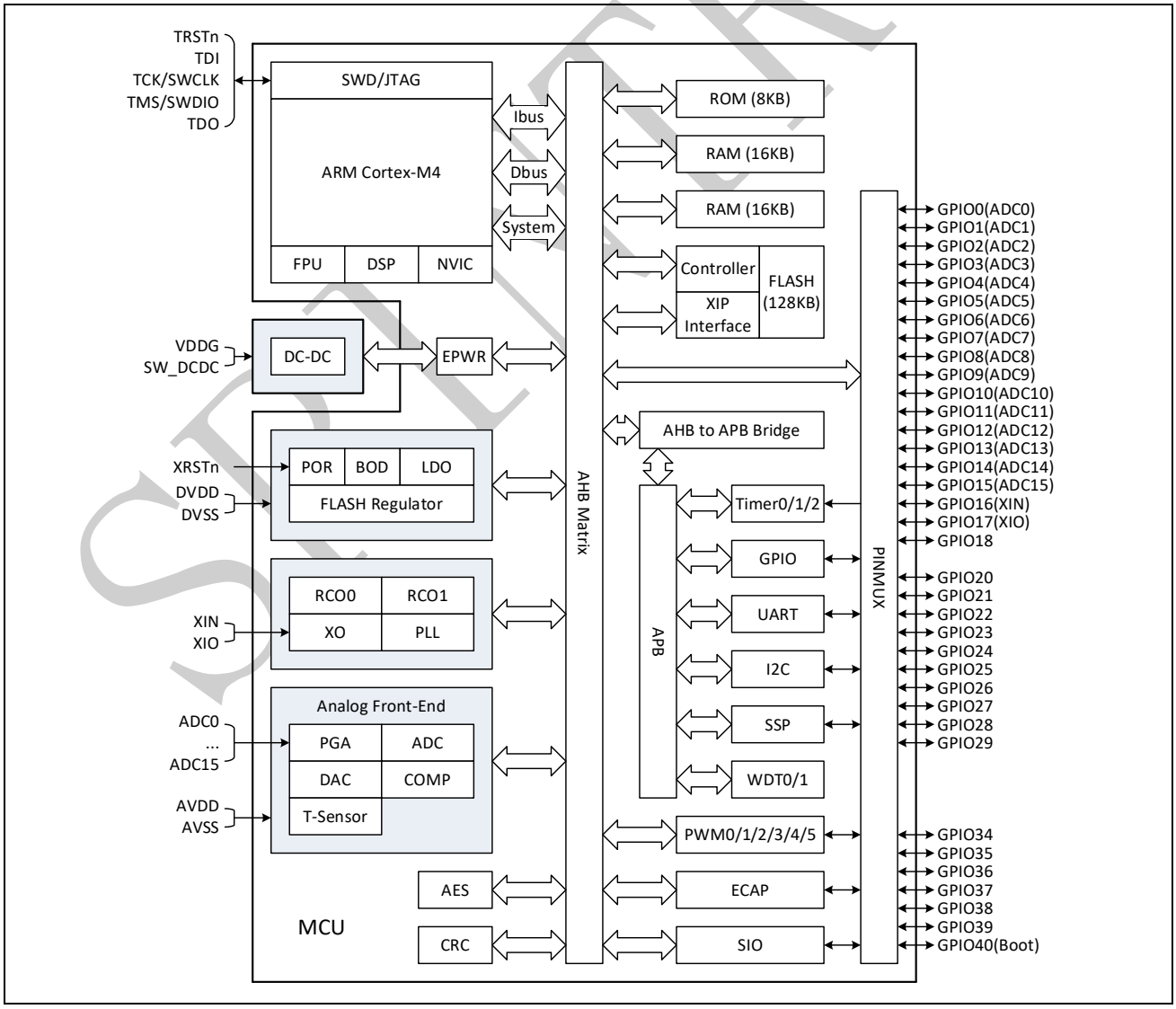
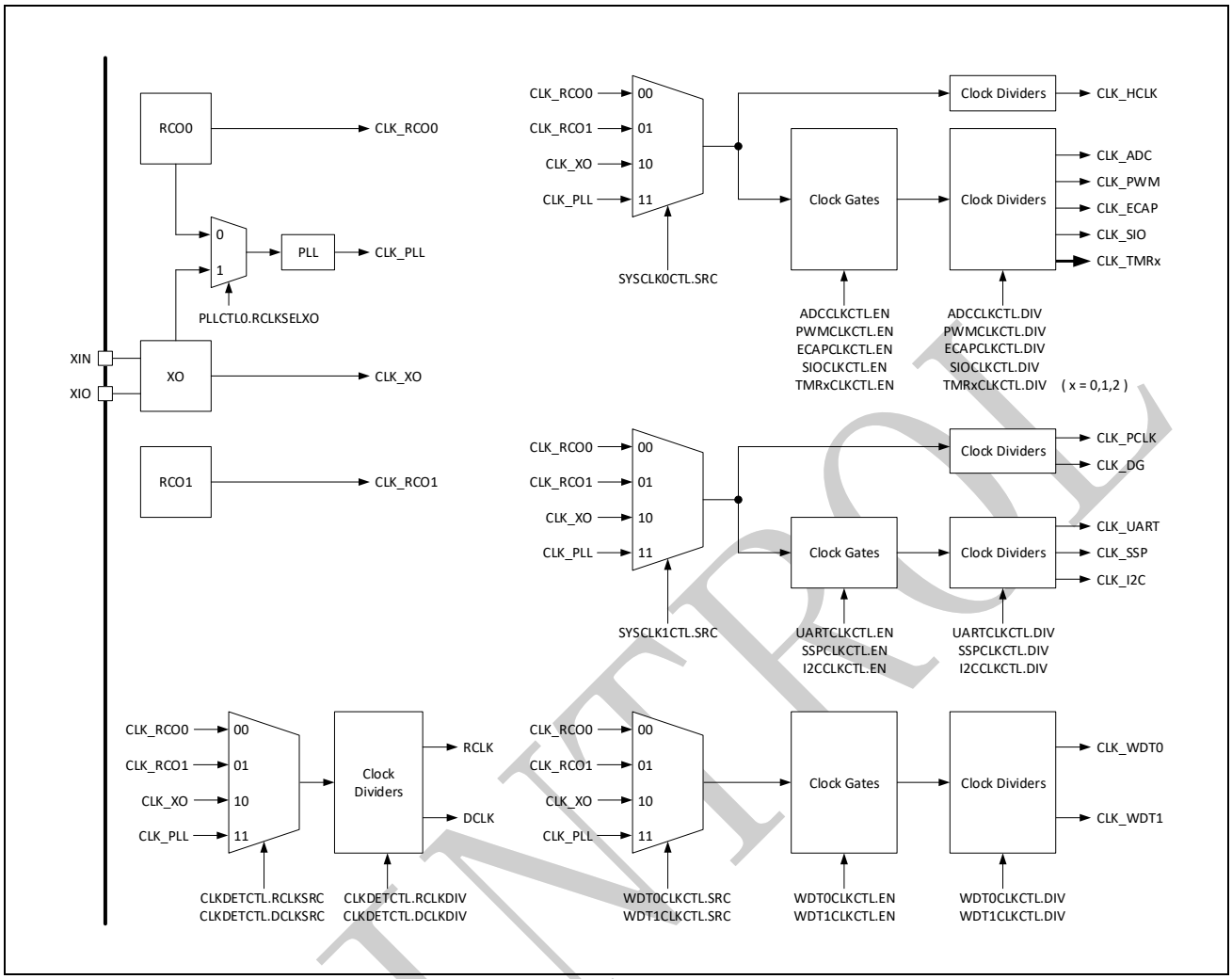


Figure 1-2: Clock tree



2 Feature descriptions

2.1 ARM Cortex-M4 core

The ARM Cortex-M4 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPC1158 integrates a full-feature ARM Cortex-M4 core with FPU that can run up to 100MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Embedded SRAM

The SPC1158 has implemented 32 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.3 Embedded Flash memory

Up to 128 KB of embedded Flash memory is available for storing programs and data.

2.4 Nested vectored interrupt controller (NVIC)

The SPC1158 embeds a nested vectored interrupt controller able to handle up to 51 mask-able interrupt channels (not including the 16 interrupt lines of Cortex-M4) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.5 External interrupt/event controller

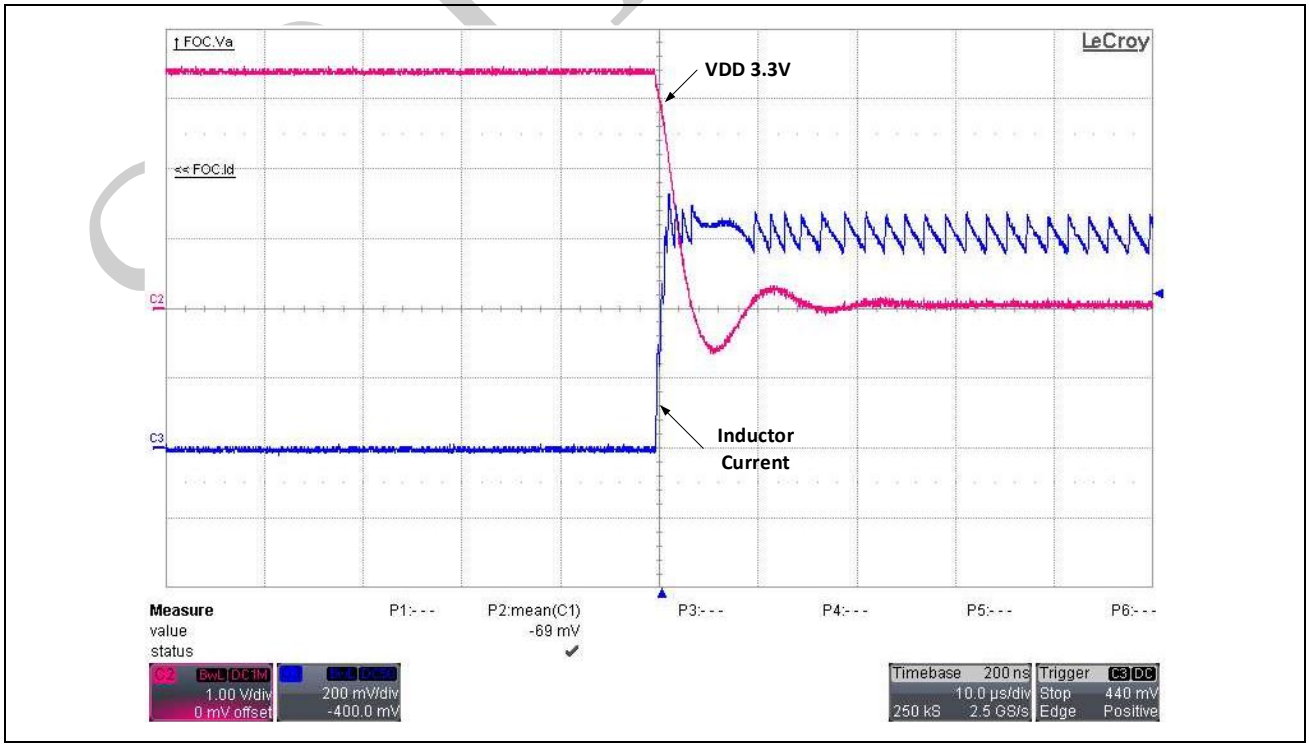
The SPC1158 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.6 Buck DC-DC, Power supply and Reset

SPC1158 integrates a buck DC-DC converter to provide 3.3V supply to MCU, with no external power FET or diode. It can also provide 3.3V supply to other circuits on the board, as long as total current out of 3.3V supply is below 500mA. The switching frequency of the buck DC-DC is programmable with options of 400 kHz, 600 kHz, 1.2 MHz, and 2.4 MHz. Optional spread-spectrum feature can be enabled for better EM performance.

- Buck DC-DC's automatic mode transition: The Buck DC-DC will automatically choose PWM mode and PFM mode for higher efficiency at light load. It also provides force PWM mode in the application where really care about supply voltage ripple.
- Buck DC-DC's current limit: The buck DC-DC will limit its output valley current to be less than 500mA. This feature is added for safety, to protect against output shorted to ground and problematic current increases which will cause chip and board reliability problems. If load valley current over 500mA is applied to the DC-DC output, the buck DC-DC will lower down its 3.3V output and operate as a 500mA valley current source. Figure 2-1 shows the inductor current and voltage behavior when 3.3V output is suddenly shorted to the ground.

Figure 2-1: The inductor current and voltage behavior



As an alternative option, SPC1158 also supports using external 3.3V supply. There are no special power-up sequence requirements for the SPC1158.

The SPC1158 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.7 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the 3.3V/1.2V domain power supply and compare it to the programmable pre-set value. An interrupt or reset can be generate when voltage of the power domain is higher or drops below the pre-set value. The interrupt service routine then generate a warning message and/or put the MCU into a safe state. The BOD is enabled by software.

2.8 Clocks

System clock selection is performed on startup. The internal 32 MHz factory-trimmed oscillator is selected by default upon reset. An external 1 – 66 MHz oscillator can be selected by the user.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal RC oscillator or external clock as the input reference clock. The output frequency covers from 25MHz to 100MHz.

Several clock dividers allow the configuration of the AHB, APB and the peripherals frequency. The maximum allowed frequency is 100MHz for AHB and 50 MHz for APB. See Figure 1-2 for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 2.2MHz backup-safety oscillator makes the SPC1158 get rid of clock stuck.

2.9 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM. The boot pin and TRSTn pin are used to select one of the two boot options:

- Boot from embedded Flash (boot pin = 1, TRSTn pin = X): the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000
- ISP mode (boot pin = 0, TRSTn pin = 0): the boot loader reprograms the embedded Flash by using UART. During the process, the GPIO34 is configured as UART_TXD and the GPIO35 is configured as UART_RXD.

Note: The boot pin should always keep high when chip normally running.
The TRSTn pin is recommended to set as low.

When TRSTn is high, the related debug interface pins (GPIO36 ~ GPIO39) must not be used as GPIO function.

2.10 General-purpose IOs (GPIOs)

The SPC1158 can be configured to support as many as 35 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter

2.11 Timers and watchdogs

The SPC1158 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPC1158 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. When the counter reaches zero, the timer can also generate an ADCSOC event or a PWMSYNC event if they are enabled. The clock of general-purpose timer can be selected from internal RC oscillators, external oscillator or PLL clock. Besides, each general-purpose timer can also capture external input as timer clock or enable signal.

Watchdogs

The SPC1158 implements two identical watchdogs. Each watchdog is based on a 32-bit down-counter, which can be clocked from internal RC oscillators, external oscillator or PLL clock. When the counter reaches the given time-out value, an interrupt or a reset can be generated. The watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

2.12 UART

The SPC1158 has an UART module. It features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5 – 8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 12.5 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

2.13 I^2C

The I^2C bus interface complies with the common I^2C protocol and can operate in standard mode (with data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s). It features:

- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.14 SPI

The SPI allows half/full-duplex, synchronous, serial communication with external devices. It features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- 50 Mbps maximum communication speed
- MSB-first data order
- Programmable clock polarity and phase
- Transmit and receive FIFOs

2.15 ADC

One 14-bit analog-to-digital convert is embedded into SPC1158 and has up to 16 external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has three independent built-in sample-and-hold (S/H). Each S/H has two input channels, which is suitable for differential sampling.

The events generated by the general-purpose timers and the PWM outputs can be internally connected to the ADC start trigger.

- 14-bit resolution
- 125 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Triple sample and hold capability
- Simultaneous sampling and sequential sampling modes supported
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external
- Input open and short detection for safety

Please see Table 5-13 for ADC characteristics.

2.16 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

2.17 PGAs

Three flexible programmable gain amplifiers (PGAs) are embedded into SPC1158 and shares up to 16 channels. The temperature sensor and internal 1.2V power can be selected as a PGA input channels. These inputs are multiplexed. Each PGA outputs are connected to ADC input channel.

- Programmable gains

  Differential mode: 2, 4, 8, 16, 24, 32, 48, 64; Single-ended mode: 1, 2, 4, 8, 12, 16, 24, 32.

- Settling time: 400 ns to 800 ns

Please see Table 5-14 for PGA characteristics.

2.18 Analog comparators

The SPC1158 has ten high-speed comparators. Each comparator use the internal DAC as reference to monitor whether the PGA inputs or outputs exceed the threshold. A DAC can be used to generate a static voltage as a threshold for the somparator, but does not guarantee the performance of the waveform. Two comparators are designed for each PGA: one is monitoring whether the voltage is too high, the other is monitoring whether the voltage is too low. The extra two pairs of comparators are reserved for additional applications. The comparator output is routed to the PWM Trip-Zone modules. Additionally, each comparator can implement the phase comparison for motor commutation. The detail channel selection can be referred to Technical Reference Manual.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter
- Phase comparison

Please see Table 5-15 and Table 5-16 for analog comparator and DAC characteristics.

2.19 PWMs

The SPC1158 integrates six PWM modules and supports 11 PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.20 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPC1158 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.21 Cyclic redundancy check (CRC)

The SPC1158 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Five CRC standard polynomials supported

2.22 Advanced encryption standard (AES) engine

The AES engine provides fast hardware encryption and decryption services. The main features are as follows:

- Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO, and Bypass
- Supports 128, 192, and 256-bits key size
- Error indication for each block cipher mode
- Separate 4 x 32-bit input and output FIFOs

2.23 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port. The SWJ-DP interface enables either a serial wire debug or a JTAG probe to be connected to the target. The debug port can be disabled when enabling SPC1158 certain security feature.

2.24 SIO

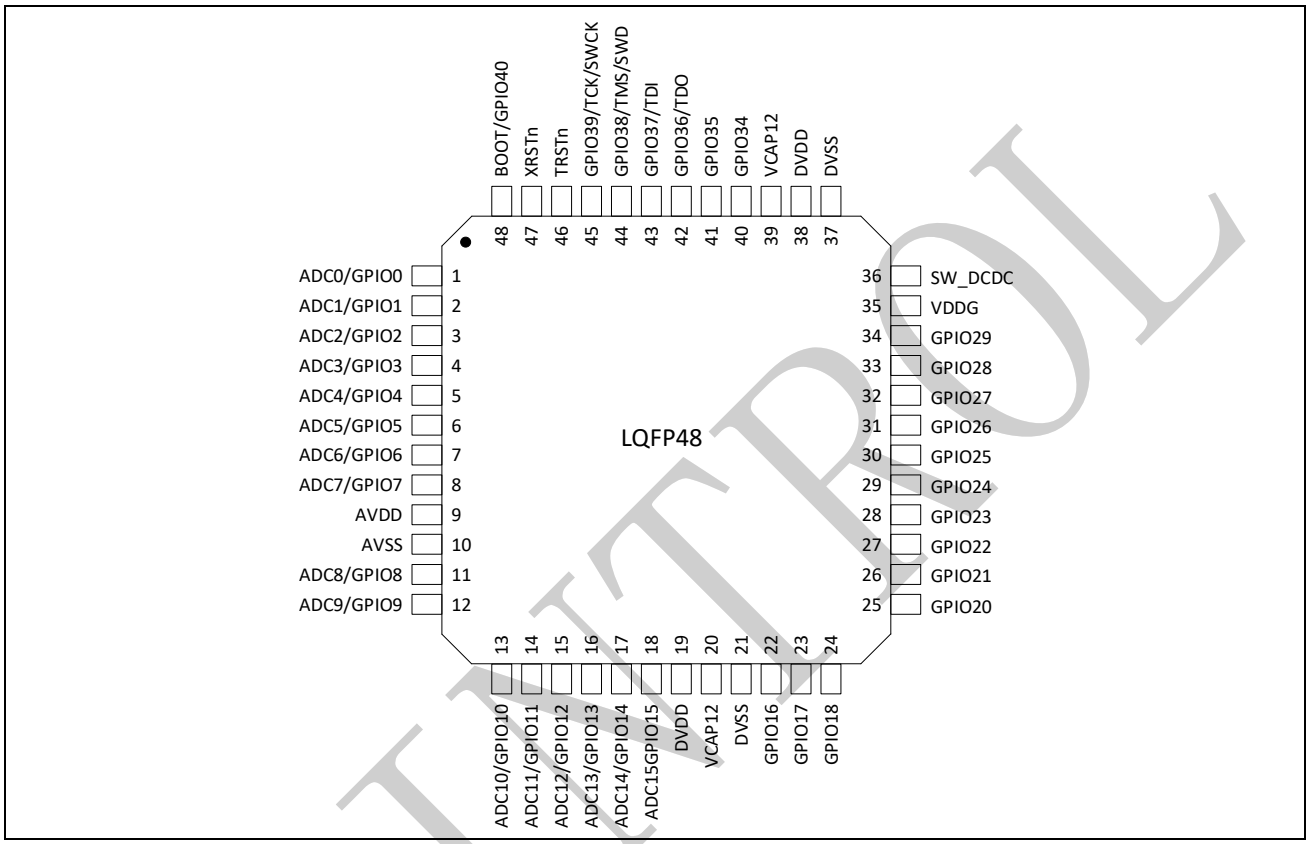
SPC1158 has implemented an SIO module, which is based on a Spintrol patented technology. It has programmable capability that can convert the SIO module into pre-defined communication module. Currently the SIO can be used as UART, SPI, I2C and CAN once it is programmed through initialization. There will be more features added in short time.

Note:	SIO is currently not supported in SPC1158(H)APE32

3 Pinouts and pin description

3.1 LQFP48

Figure 3-1: SPC1158 LQFP48 pinout



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO36 ~ GPIO39 pins work as Debug interface and can't be configured as other functions.

Table 3-1: SPC1158 LQFP48 pin definitions

Pin	Signal	Type(1)	Description
1	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
2	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
3	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input

Pin	Signal	Type(1)	Description
	COMP1H	O	Comparator COMP1H result output
4	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
5	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
6	GPIO5	I/O	General-purpose input/output 5
	ADC5	AI	ADC channel 5 input
	COMP2L	O	Comparator COMP2L result output
7	GPIO6	I/O	General-purpose input/output 6
	ADC6	AI	ADC channel 6 input
8	GPIO7	I/O	General-purpose input/output 7
	ADC7	AI	ADC channel 7 input
9	AVDD	S	Analog power, **series 0 Ohm resistor to DVDD and add 2.2uF and 0.1uF bypass ceramic cap to AVSS near pin**
10	AVSS	S	Analog ground
11	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output
	PWMSOC	O	PWM SOC signal output for monitoring
12	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
	COMP3L	O	Comparator COMP3L result output
13	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output

Pin	Signal	Type[1]	Description
	COMP4H	O	Comparator COMP4H result output
14	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master out, slave input
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO[2]	O	Trip-zone signal from ePower module for monitoring
15	GPIO12	I/O	General-purpose input/output 12
	ADC12	AI	ADC channel 12 input
	I2C_SCL	I/O	I^2C clock
16	GPIO13	I/O	General-purpose input/output 13
	ADC13	AI	ADC channel 13 input
	I2C_SDA	I/O	I^2C data
17	GPIO14	I/O	General-purpose input/outpu14
	ADC14	AI	ADC channel 14 input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
18	GPIO15	I/O	General-purpose input/output 5
	ADC15	AI	ADC channel 15 input
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
19	DVDD	S	Digital power, **add 10uF and 0.1uF bypass ceramic cap to DVSS**
20	VCAP12	S	1.2V power, **add 2.2uF bypass ceramic cap to DVSS**
21	DVSS	S	Digital ground
22	GPIO16	I/O	General-purpose input/output 16
	XIN	AI	External oscillator input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWM2A	O	PWM2 output A

Pin	Signal	Type(1)	Description
	PWM5A	O	PWM5 output A
	SIO0_12	I/O	SIO0 input/output 12
23	GPIO17	I/O	General-purpose input/output 17
	XIO	AI/O	External oscillator input/output
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWM2B	O	PWM2 output B
	PWM5B	O	PWM5 output B
	SIO0_13	I/O	SIO0 input/output 13
24	GPIO18	I/O	General-purpose input/output 18
	PWM3A	O	PWM3 output A
	COMP3H	O	Comparator COMP3H result output
	PWM0A	O	PWM0 output A
	SIO0_14	I/O	SIO0 input/output 14
25	GPIO20	I/O	General-purpose input/output 20
	COMP4H	O	Comparator COMP4H result output
	PWM2A	O	PWM2 output A
	PWM1A	O	PWM1 output A
	SIO0_16	I/O	SIO0 input/output 16
26	GPIO21	I/O	General-purpose input/output 21
	COMP4L	O	Comparator COMP4L result output
	PWM0B	O	PWM0 output B
	PWM1B	O	PWM1 output B
	SIO0_17	I/O	SIO0 input/output 17
27	GPIO22	I/O	General-purpose input/output 22
	PWM1B	O	PWM1 output B
	PWM2A	O	PWM2 output A
	SIO0_0	I/O	SIO0 input/output 0
28	GPIO23	I/O	General-purpose input/output 23
	PWM2B	O	PWM2 output B
	SIO0_1	I/O	SIO0 input/output 1

Pin	Signal	Type(1)	Description
29	GPIO24	I/O	General-purpose input/output 24
	COMP0H	O	Comparator COMP0H result output
	PWM3A	O	PWM3 output A
	SIO0_2	I/O	SIO0 input/output 2
30	GPIO25	I/O	General-purpose input/output 25
	COMP0L	O	Comparator COMP0L result output
	PWM4A	O	PWM4 output A
	PWM3B	O	PWM3 output B
	SIO0_3	I/O	SIO0 input/output 3
31	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output
	PWM5A	O	PWM5 output A
	PWM4A	O	PWM4 output A
	SIO0_4	I/O	SIO0 input/output 4
32	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM3B	O	PWM3 output B
	PWM4B	O	PWM4 output B
	SIO0_5	I/O	SIO0 input/output 5
33	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM4B	O	PWM4 output B
	PWM5A	O	PWM5 output A
	SIO0_6	I/O	SIO0 input/output 6
34	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM5B	O	PWM5 output B
	SIO0_7	I/O	SIO0 input/output 7
35	VDDG	S	7~20V power input, **add at least 2.2uF bypass ceramic cap to DVSS**

Pin	Signal	Type(1)	Description
36	SW_DCDC	S	DC-DC's switching node, **add 10uH inductor to DVDD**. The saturate current for inductor should be larger than 500mA.
37	DVSS	S	Digital ground
38	DVDD	S	Digital power, **add 10uF and 0.1uF bypass ceramic cap to DVSS**
39	VCAP12	S	1.2V power, **add 0.1uF bypass ceramic cap to DVSS**
40	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	SIO0_12	I/O	SIO0 input/output 12
41	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	SIO0_13	I/O	SIO0 input/output 13
42	GPIO36	I/O	General-purpose input/output 36
	TDO	O	JTAG data output
	UART_RXD	I	UART receive data
	SPI_SCLK	I/O	SPI clock input/output
	PWM5A	O	PWM5 output A
	PWM1A	O	PWM1 output A
	SIO0_14	I/O	SIO0 input/output 14
	Note: when TRSTn is HIGH, this pin always works as TDO and can't be configured as other functions.		
43	GPIO37	I/O	General-purpose input/output 37
	TDI	I	JTAG data input

Pin	Signal	Type(1)	Description
	UART_TXD	O	UART transmit data
	SPI_SFRM	I/O	SPI frame signal
	PWM5B	O	PWM5 output B
	PWM1B	O	PWM1 output B
	SIO0_15	I/O	SIO0 input/output 15
	Note: when TRSTn is HIGH, this pin always works as TDI and can't be configured as other functions.		
44	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	SIO0_16	I/O	SIO0 input/output 16
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
45	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG clock or SWD clock
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	SIO0_17	I/O	SIO0 input/output 17
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
46	TRSTn	I	JTAG reset pin, reset the JTAG when low
47	XRSTn	I	Device reset pin, reset the device when low
48	BOOT(GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	DCLK	O	Clock output from CLKDET module for monitoring

Pin	Signal	Type[1]	Description
	EPWRTZ1O[2]	O	Trip-zone signal 1 from ePower module for monitoring
	SIO0_0	I/O	SIO0 input/output 0

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

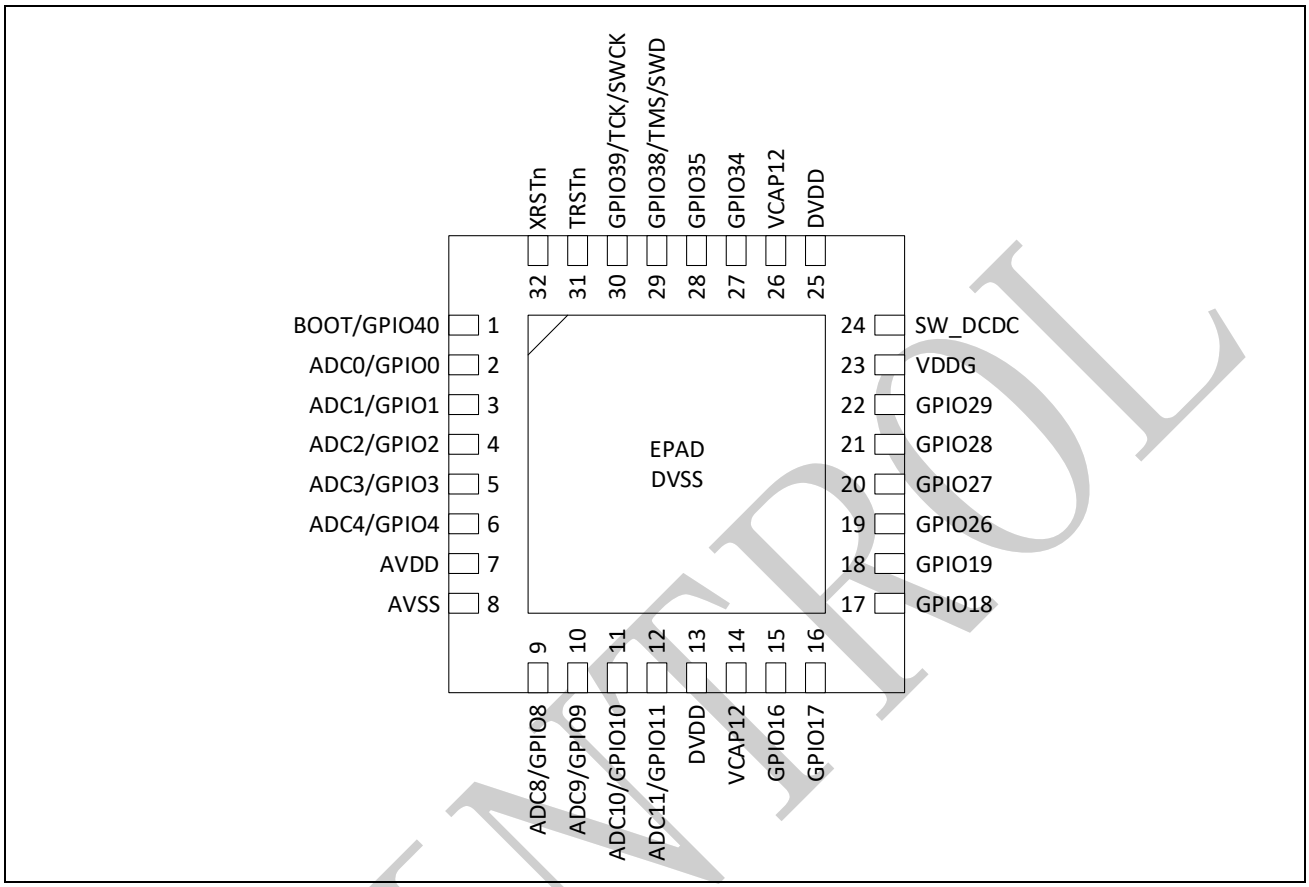
[2] The value of EPWRTZO and EPWRTZ1O are the same in SPC1158。

[3] All GPIO pins can be configured as ECAP input.

[4] All GPIO pins (except GPIO36 and GPIO37) can be configured as ECAP output.

3.2 QFN32

Figure 3-2: SPC1158 QFN32 pinout



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO38 ~ GPIO39 pins work as Debug interface and can't be configured as other functions.

Table 3-2: SPC1158 QFN32 pin definitions

Pin	Signal	Type(1)	Description
1	BOOT(GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	SIO0_0	I/O	SIO0 input/output 0
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZ1O(2)	O	Trip-zone signal 1 from ePower module for monitoring
2	GPIO0	I/O	General-purpose input/output 0
	ADC0	AI	ADC channel 0 input

Pin	Signal	Type(1)	Description
	COMP0H	O	Comparator COMP0H result output
3	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
4	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
5	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
6	GPIO4	I/O	General-purpose input/output 4
	ADC4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
7	AVDD	S	Analog power, **series 0 Ohm resistor to DVDD and add 2.2uF and 0.1uF bypass ceramic cap to AVSS near pin**
8	AVSS	S	Analog ground
9	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output
	PWMSOC	O	PWM SOC signal output for monitoring
10	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
	COMP3L	O	Comparator COMP3L result output
11	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output

Pin	Signal	Type[1]	Description
12	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO[2]	O	Trip-zone signal from ePower module for monitoring
13	DVDD	S	Digital power, **add 10uF and 0.1uF bypass ceramic cap to DVSS**
14	VCAP12	S	1.2V power, **add 2.2uF bypass ceramic cap to DVSS**
15	GPIO16	I/O	General-purpose input/output 16
	XIN	AI	External oscillator input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWM2A	O	PWM2 output A
	PWM5A	O	PWM5 output A
	SIO0_12	I/O	SIO0 input/output 12
16	GPIO17	I/O	General-purpose input/output 17
	XIO	AI/O	External oscillator input or output
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	PWM2B	O	PWM2 output B
	PWM5B	O	PWM5 output B
	SIO0_13	I/O	SIO0 input/output 13
17	GPIO18	I/O	General-purpose input/output 18
	PWM3A	O	PWM3 output A
	COMP3H	O	Comparator COMP3H result output
	PWM0A	O	PWM0 output A
	SIO0_14	I/O	SIO0 input/output 14
18	GPIO19	I/O	General-purpose input/output 19
	PWM4A	O	PWM4 output A

Pin	Signal	Type(1)	Description
	PWM3B	O	PWM3 output B
	COMP3L	O	Comparator COMP3L result output
	PWM1A	O	PWM1 output A
	PWM0B	O	PWM0 output B
	SIO0_15	I/O	SIO0 input/output 15
19	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output
	PWM5A	O	PWM5 output A
	PWM4A	O	PWM4 output A
	SIO0_4	I/O	SIO0 input/output 4
20	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM3B	O	PWM3 output B
	PWM4B	O	PWM4 output B
	SIO0_5	I/O	SIO0 input/output 5
21	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM4B	O	PWM4 output B
	PWM5A	O	PWM5 output A
	SIO0_6	I/O	SIO0 input/output 6
22	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM5B	O	PWM5 output B
	SIO0_7	I/O	SIO0 input/output 7
23	VDDG	S	7~20V power input, **add at least 2.2uF bypass ceramic cap to DVSS**
24	SW_DCDC	S	DC-DC's switching node, **add 10uH inductor to DVDD**. The saturate current for inductor should be larger than 500mA.
25	DVDD	S	Digital power, **add 10uF and 0.1uF bypass ceramic cap to DVSS**
26	VCAP12	S	1.2V power, **add 0.1uF bypass ceramic cap to DVSS**

Pin	Signal	Type(1)	Description
27	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	SIO0_12	I/O	SIO0 input/output 12
28	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	SIO0_13	I/O	SIO0 input/output 13
29	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	SIO0_16	I/O	SIO0 input/output 16
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
30	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG clock or SWD clock
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	SIO0_17	I/O	SIO0 input/output 17

Pin	Signal	Type[1]	Description
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
31	TRSTn	I	JTAG reset pin, reset the JTAG when low
32	XRSTn	I	Device reset pin, reset the device when low

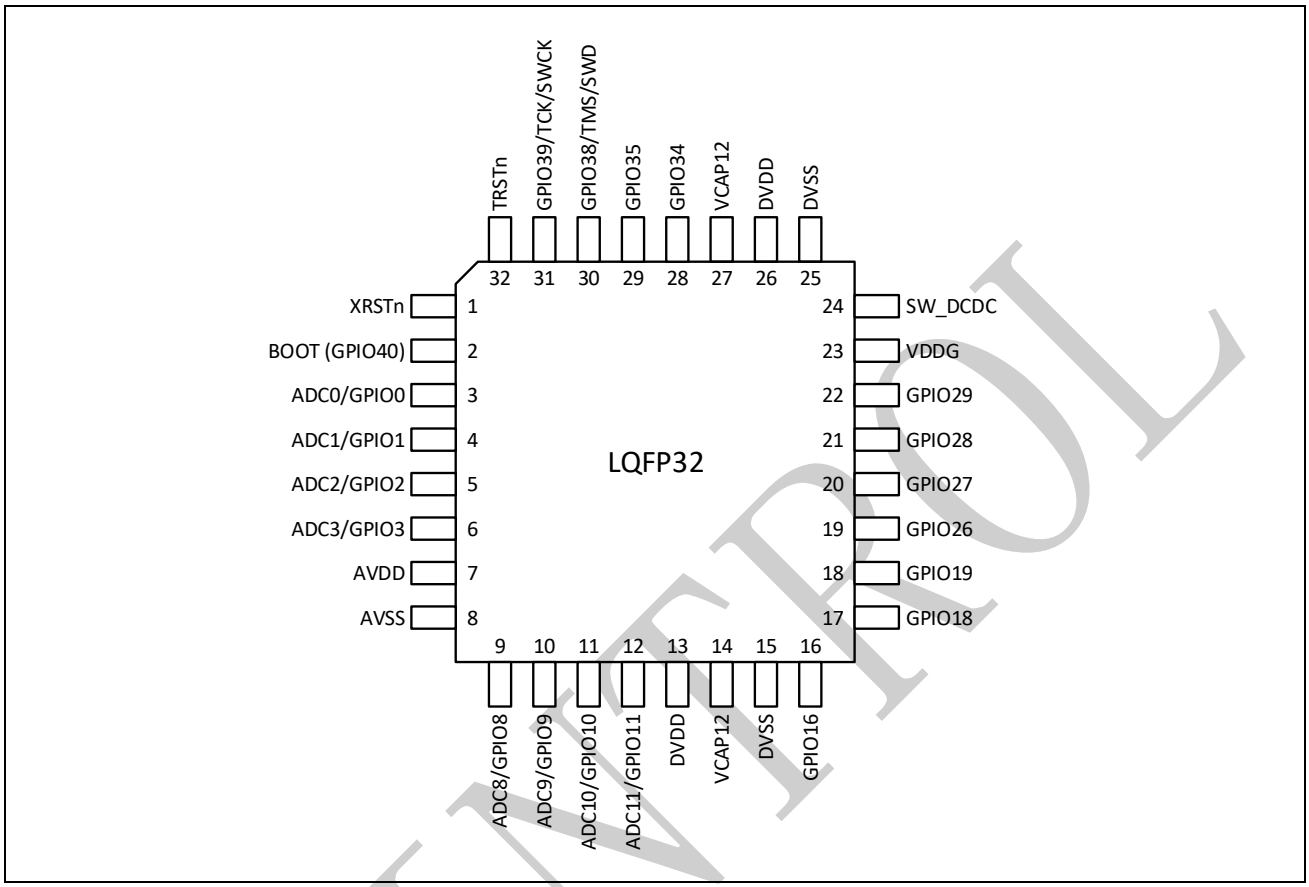
[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] The value of EPWRTZO and EPWRTZ1O are the same in SPC1158.

[3] All GPIO pins can be configured as ECAP input and output.

3.3 LQFP32

Figure 3-3: SPC1158 LQFP32 pinout



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO38 ~ GPIO39 pins work as Debug interface and can't be configured as other functions.

Table 3-3: SPC1158 LQFP32 pin definitions

Pin	Signal	Type(1)	Description
1	XRSTn	I	Device reset pin, reset the device when low
2	BOOT(GPIO40)	I/O	Boot pin (General-purpose input/output 40)
	SPI_SCLK	I/O	SPI clock input/output
	UART_TXD	O	UART transmit data
	SIO0_0	I/O	SIO0 input/output 0
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZ1O(2)	O	Trip-zone signal 1 from ePower module for monitoring
3	GPIO0	I/O	General-purpose input/output 0

Pin	Signal	Type(1)	Description
	ADC0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
4	GPIO1	I/O	General-purpose input/output 1
	ADC1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
5	GPIO2	I/O	General-purpose input/output 2
	ADC2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
6	GPIO3	I/O	General-purpose input/output 3
	ADC3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
7	AVDD	S	Analog power, **series 0 Ohm resistor to DVDD and add 2.2uF and 0.1uF bypass ceramic cap to AVSS near pin**
8	AVSS	S	Analog ground
9	GPIO8	I/O	General-purpose input/output 8
	ADC8	AI	ADC channel 8 input
	SPI_SCLK	I/O	SPI clock input/output
	COMP3H	O	Comparator COMP3H result output
	PWMSOC	O	PWM SOC signal output for monitoring
10	GPIO9	I/O	General-purpose input/output 9
	ADC9	AI	ADC channel 9 input
	SPI_SFRM	I/O	SPI frame signal
	COMP3L	O	Comparator COMP3L result output
11	GPIO10	I/O	General-purpose input/output 10
	ADC10	AI	ADC channel 10 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP4H	O	Comparator COMP4H result output
12	GPIO11	I/O	General-purpose input/output 11
	ADC11	AI	ADC channel 11 input

Pin	Signal	Type[1]	Description
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	COMP4L	O	Comparator COMP4L result output
	DCLK	O	Clock output from CLKDET module for monitoring
	EPWRTZO[2]	O	Trip-zone signal from ePower module for monitoring
13	DVDD	S	Digital power, **add 10uF and 0.1uF bypass ceramic cap to DVSS**
14	VCAP12	S	1.2V power, **add 2.2uF bypass ceramic cap to DVSS**
15	DVSS	S	Digital ground
16	GPIO16	I/O	General-purpose input/output 16
	XIN	AI	External oscillator input
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	PWM2A	O	PWM2 output A
	PWM5A	O	PWM5 output A
	SIO0_12	I/O	SIO0 input/output 12
17	GPIO18	I/O	General-purpose input/output 18
	PWM3A	O	PWM3 output A
	COMP3H	O	Comparator COMP3H result output
	PWM0A	O	PWM0 output A
	SIO0_14	I/O	SIO0 input/output 14
18	GPIO19	I/O	General-purpose input/output 19
	PWM4A	O	PWM4 output A
	PWM3B	O	PWM3 output B
	COMP3L	O	Comparator COMP3L result output
	PWM1A	O	PWM1 output A
	PWM0B	O	PWM0 output B
	SIO0_15	I/O	SIO0 input/output 15
19	GPIO26	I/O	General-purpose input/output 26
	COMP1H	O	Comparator COMP1H result output
	PWM5A	O	PWM5 output A

Pin	Signal	Type(1)	Description
	PWM4A	O	PWM4 output A
	SIO0_4	I/O	SIO0 input/output 4
20	GPIO27	I/O	General-purpose input/output 27
	COMP1L	O	Comparator COMP1L result output
	PWM3B	O	PWM3 output B
	PWM4B	O	PWM4 output B
	SIO0_5	I/O	SIO0 input/output 5
21	GPIO28	I/O	General-purpose input/output 28
	COMP2H	O	Comparator COMP2H result output
	PWM4B	O	PWM4 output B
	PWM5A	O	PWM5 output A
	SIO0_6	I/O	SIO0 input/output 6
22	GPIO29	I/O	General-purpose input/output 29
	COMP2L	O	Comparator COMP2L result output
	PWM5B	O	PWM5 output B
	SIO0_7	I/O	SIO0 input/output 7
23	VDDG	S	7~20V power input, **add at least 2.2uF bypass ceramic cap to DVSS**
24	SW_DCDC	S	DC-DC's switching node, **add 10uH inductor to DVDD**. The saturate current for inductor should be larger than 500mA.
25	DVSS	S	Digital ground
26	DVDD	S	Digital power, **add 10uF and 0.1uF bypass ceramic cap to DVSS**
27	VCAP12	S	1.2V power, **add 0.1uF bypass ceramic cap to DVSS**
28	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	SIO0_12	I/O	SIO0 input/output 12

Pin	Signal	Type[1]	Description
29	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	SIO0_13	I/O	SIO0 input/output 13
30	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	I2C_SDA	I/O	I^2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	SIO0_16	I/O	SIO0 input/output 16
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		
31	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG clock or SWD clock
	I2C_SCL	I/O	I^2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	SIO0_17	I/O	SIO0 input/output 17
	Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
32	TRSTn	I	JTAG reset pin, reset the JTAG when low

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] The value of EPWRTZO and EPWRTZ1O are the same in SPC1158.

[3] All GPIO pins can be configured as ECAP input and output.

3.4 PGA input channel selection

For the three on-MCU PGA's, each PGA has two 1-of-8 multiplexers (MUX) for input channel selection, one is for positive input (PGAx_P, x = 0,1,2) and the other is for negative input (PGAx_N, x = 0,1,2). The input channel selection table is shown below.

Table 3-4: PGA input channel selection

MUX Value	PGA0_P	PGA0_N	PGA1_P	PGA1_N	PGA2_P	PGA2_N
7	ADC4	ADC3	ADC9	ADC1	ADC14	ADC15
6	ADC10	ADC5	ADC10	ADC11	ADC12	ADC13
5	ADC8	ADC9	ADC8	ADC10	ADC8	ADC11
4	ADC6	ADC7	ADC2	ADC3	ADC4	ADC5
3	ADC0	ADC1	ADC0	ADC2	ADC0	ADC3
2	DAC2	DAC3	ATEST	VDD12	TSEN1[1]	TSEN0[1]
1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
0	GND	GND	GND	GND	GND	GND

[1] TSEN0 is output 0 of T-Sensor and TSEN1 is output 1 of T-Sensor.

3.5 GPIO pin function and state after reset

Table 3-5: GPIO pin function and state after reset

Pin Name	Default Function	Default State
GPIO0	ADC0	Floating
GPIO1	ADC1	Floating
GPIO2	ADC2	Floating
GPIO3	ADC3	Floating
GPIO4	ADC4	Floating
GPIO5	ADC5	Floating
GPIO6	ADC6	Floating
GPIO7	ADC7	Floating
GPIO8	ADC8	Floating
GPIO9	ADC9	Floating
GPIO10	ADC10	Floating
GPIO11	ADC11	Floating
GPIO12	ADC12	Floating
GPIO13	ADC13	Floating
GPIO14	ADC14	Floating
GPIO15	ADC15	Floating
GPIO16	GPIO16	Floating
GPIO17	GPIO17	Floating
GPIO18	GPIO18	Floating
GPIO19	GPIO19	Floating
GPIO20	GPIO20	Floating
GPIO21	GPIO21	Floating
GPIO22	GPIO22	Floating
GPIO23	GPIO23	Floating
GPIO24	GPIO24	Floating
GPIO25	GPIO25	Floating
GPIO26	GPIO26	Floating
GPIO27	GPIO27	Floating

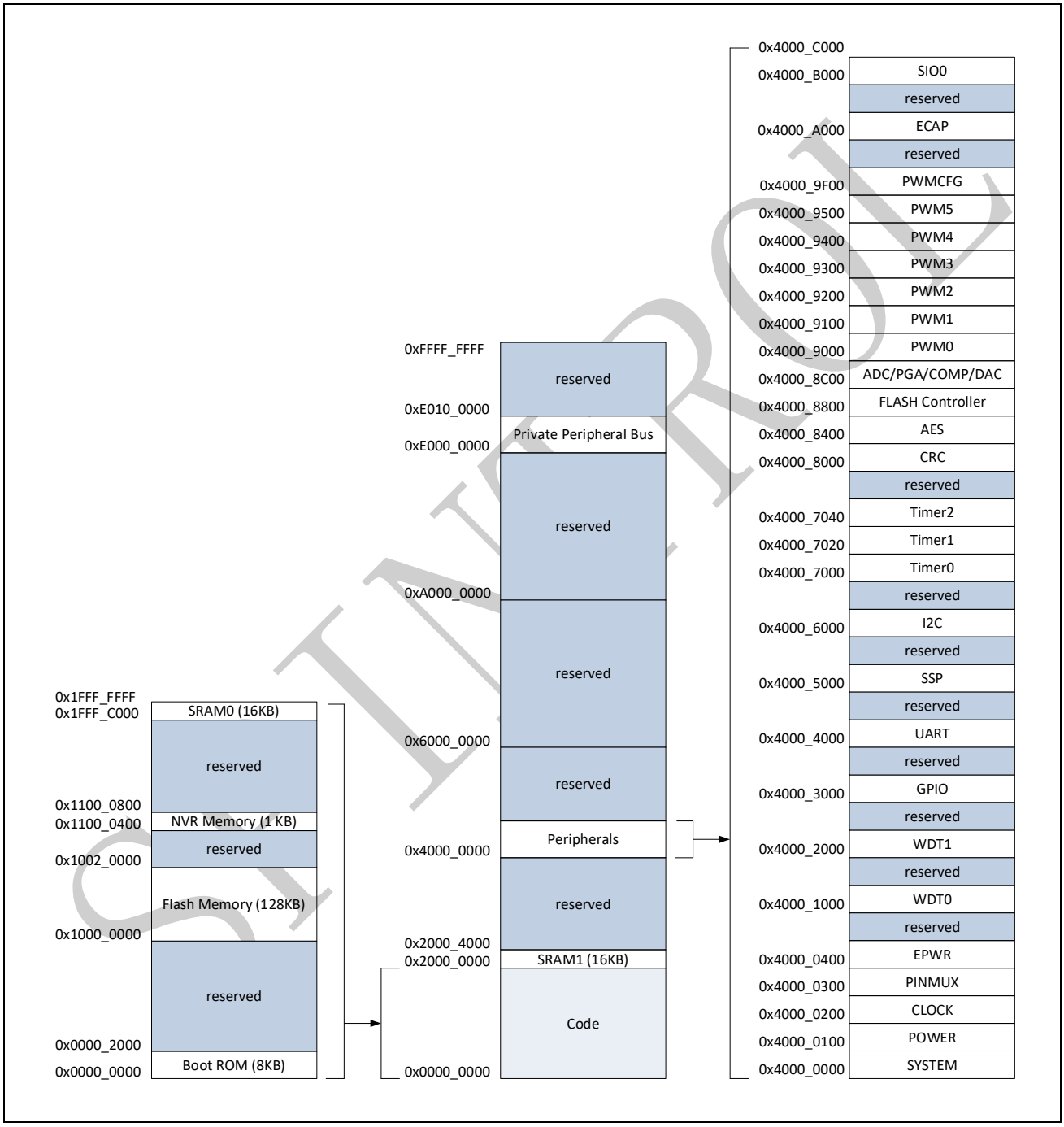
Pin Name	Default Function	Default State
GPIO28	GPIO28	Floating
GPIO29	GPIO29	Floating
~~GPIO30~~	~~GPIO30~~	Floating
~~GPIO31~~	~~GPIO31~~	Floating
~~GPIO32~~	~~GPIO32~~	Floating
~~GPIO33~~	~~GPIO33~~	Floating
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up
GPIO36	GPIO36	Floating
GPIO37	GPIO37	Floating
GPIO38	GPIO38	Floating
GPIO39	GPIO39	Floating
GPIO40	GPIO40/BOOT	Pull up

[1] The GPIOs with strikeout are not bonded out to the external pin in SPC1158.

4 Memory mapping

The memory map of SPC1158 is shown in Figure 4-1.

Figure 4-1: Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DDG}	Buck DC-DC supply voltage, with respect to V_{SS}	-0.3	22	V
I_{BUCK_VALLY}	Buck output valley current	-	500	mA
V_{DD}	Supply voltage, with respect to V_{SS}	-0.3	4.6	V
V_{DDA}	Analog voltage, with respect to V_{SSA}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DD} = 3.3 V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature(3)	-40	+125	°C
T_A	Ambient temperature(3)	-40	+105	°C
T_{stg}	Storage temperature(3)	-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

[2] All voltage values are with respect to V_{SS}, unless otherwise noted.

[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DDG}	Buck DC-DC supply voltage			15	20	V
V_{DD}	Supply voltage	-	2.97	3.3	3.63	V
V_{SS}	Supply ground	-	-	0	-	V
V_{DDA}	Analog supply voltage	-	2.97	3.3	3.63	V
V_{SSA}	Analog ground	-	-	0	-	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
T_J	Junction temperature	-	-40	-	+125	°C
T_A	Ambient temperature	-	-40	-	+105	°C

5.3 I/O Electrical characteristics

Table 5-3: I/O Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	V_{DD}-0.4	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	-	-	0.4	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.0	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	-	-	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V V_{IH} = 0 V	-	-	2	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down disabled)	V_{DD} = 3.3V V_{IH} = V_{DD}	-	-	2	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	-	41	-	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DD}	-	42	-	kΩ

5.4 Buck DCDC characteristics

Table 5-4: DCDC switching regulator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$VDDG_{UVT}$	VDDG under voltage trigger threshold	-	-	6.2	-	V
$VDDG_{UVR}$	VDDG under voltage release threshold	-	-	6.4	-	V
VSW_{DCDC}	DC/DC output voltage	-	3.15	3.3	3.45	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{SW}	DC/DC Switching Frequency	1.2MHz option	880	1157	1520	kHz
R_{DSON_HS}	DC/DC high side Ron	-	-	1.1	-	Ω
R_{DSON_LS}	DC/DC low side Ron	-	-	0.4	-	Ω
η	Efficiency	200mA@V_{DDG}=15V	-	89	-	%
I_{LIMIT}	Current limit threshold	-	-	500	-	mA

Figure 5-1: DCDC switching regulator efficiency (TA = 25 °C)

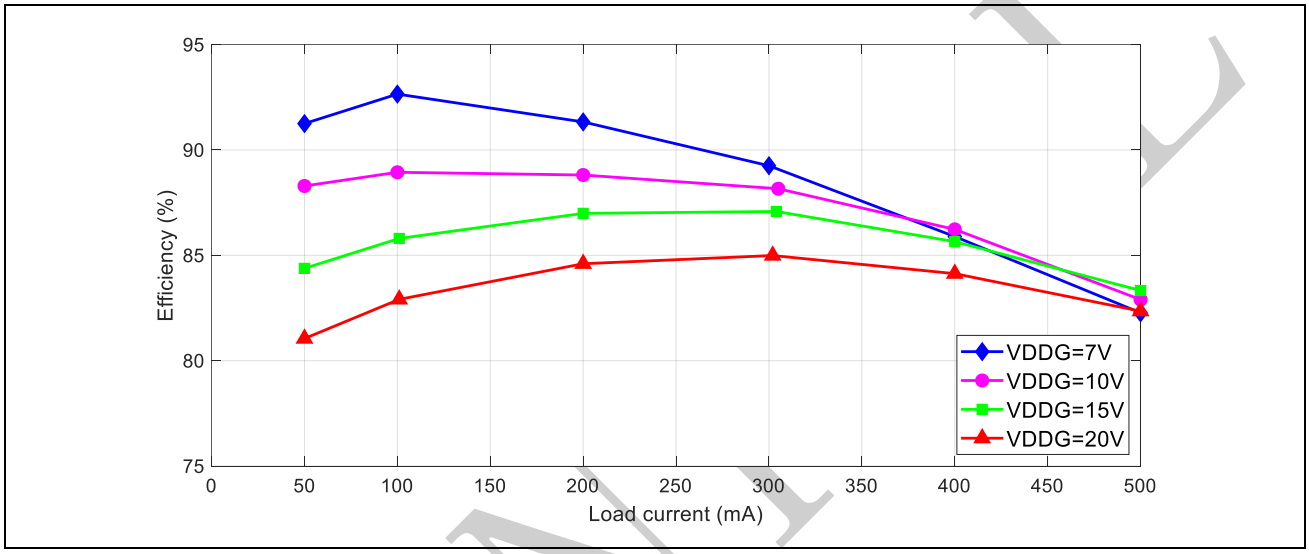
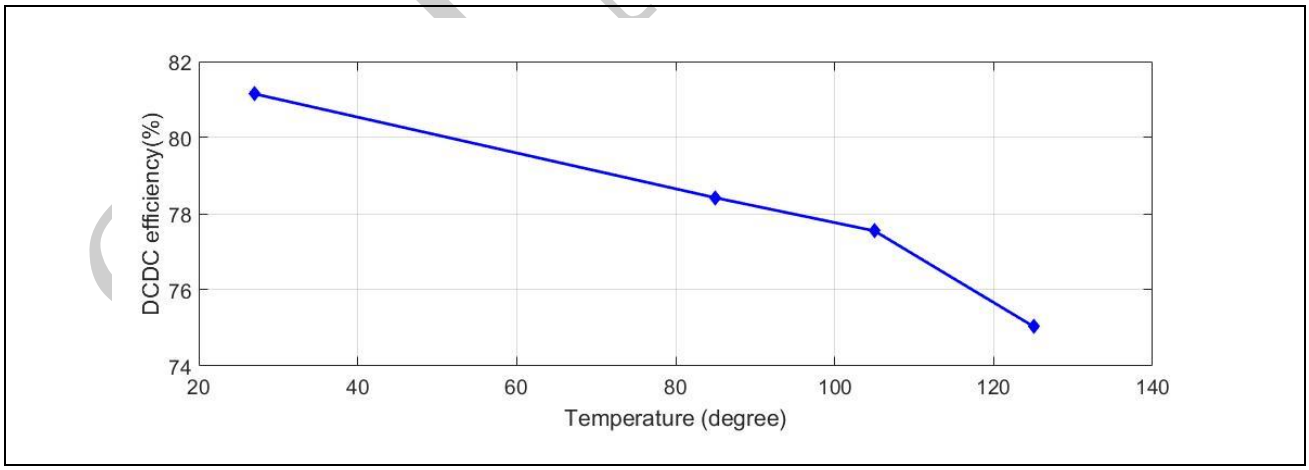


Figure 5-2: DCDC switching regulator efficiency with different temperature (VDD33 with 500mA loading)



5.5 Power consumption summary

Typical current consumption

In operational mode, the SPC1158 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are enabled;
- All peripheral clocks are as fast as HCLK (frequency division is 1), except SSP (Max 50 MHz) I2C (Max 50 MHz), PCLK (Max 50 MHz) and DGCLK (Max 50 MHz);
- All clock modules are enabled;
- Select PLL clock as system clock source.

In idle mode, the SPC1158 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO0 and XO) are disabled;
- Select RCO1 as system clock source.

In deep sleep mode, the SPC1158 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO1 and XO) are disabled;
- 1.2V LDO is shut down to 0V.

The typical current consumption of SPC1158 measured from 15V VDDG is shown in Table 5-5 and Table 5-6. The operational current consumption over various HCLK frequency is shown in Figure 5-3.

Table 5-5: SPC1158 typical current consumption (Run in FLASH)

Mode	Conditions			Typ	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}		
Operational	100 MHz	50 MHz	100 MHz	15.436	mA
	90 MHz	45MHz	90 MHz	15.077	mA
	80 MHz	40 MHz	80 MHz	14.683	mA
	70 MHz	35 MHz	70 MHz	14.224	mA
	60 MHz	30 MHz	60 MHz	13.762	mA
	50 MHz	50 MHz	50 MHz	13.477	mA
	40 MHz	40 MHz	40 MHz	12.978	mA

Mode	Conditions			Typ	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}		
	32 MHz	32 MHz	32 MHz	12.624	mA
	25 MHz	25 MHz	25 MHz	12.245	mA
Idle	2.2 MHz	2.2 MHz	-	1.619	mA
Deep Sleep	-	-	-	0.520	mA

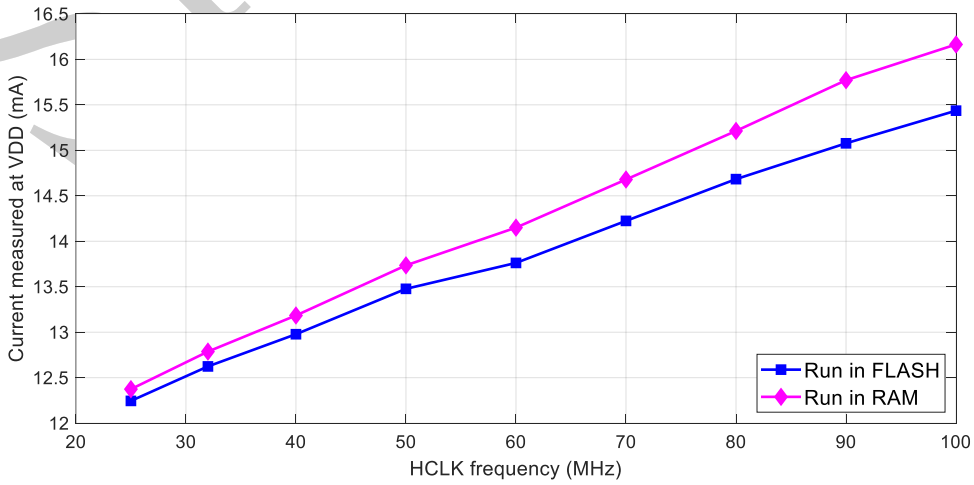
[1] Typical values are measured at T_A = 25 °C, V_{DDG} = 15 V, V_{DD} = 3.3 V.

Table 5-6: SPC1158 typical current consumption (Run in RAM)

Mode	Conditions			Typ	Unit
	f_{HCLK}	f_{PCLK}	f_{PLL}		
Operational	100 MHz	50 MHz	100 MHz	16.164	mA
	90 MHz	45MHz	90 MHz	15.771	mA
	80 MHz	40 MHz	80 MHz	15.213	mA
	70 MHz	35 MHz	70 MHz	14.679	mA
	60 MHz	30 MHz	60 MHz	14.150	mA
	50 MHz	50 MHz	50 MHz	13.735	mA
	40 MHz	40 MHz	40 MHz	13.184	mA
	32 MHz	32 MHz	32 MHz	12.787	mA
	25 MHz	25 MHz	25 MHz	12.374	mA
Idle	2.2 MHz	2.2 MHz	-	1.644	mA

[1] Typical values are measured at T_A = 25 °C, V_{DDG} = 15 V, V_{DD} = 3.3 V.

Figure 5-3: Typical operational current versus frequency



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 5-7. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO0 and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
- With all peripherals clocked disabled
- With only one peripheral enabled

Table 5-7: Peripheral current consumption

Peripherals(1)		Conditions	Typ(2)	Unit
BOD		Select RCO0 as system clock source; All other peripherals are in default settings; Close PLL, XO, RCO1 and RCO0 after disabling or enabling BOD module	25.88	uA
ADC	Analog(3)	Select PLL clock as system clock source; All peripheral clocks are set to the maximum; f_{HCLK} = 100 MHz, f_{PCLK} = 50 MHz, f_{PLL} = 100 MHz	4.275	mA
	Digital		62.68	uA
T-Sensor			41.41	uA
PGA(4)			1.061	mA
DAC			46.58	uA
Comparator			2.071	uA
UART		UART clock 100MHz, 256000 bps	58.07	uA
I2C		I2C clock 50MHz, 3.4Mbps	68.18	uA
SSP		SSP clock 50MHz, 50Mbps	74.74	uA
PWM		PWM clock 100MHz	153.3	uA
ECAP		ECAP clock 100MHz	40.81	uA
WDT		WDT clock 100MHz	30.59	uA
TMR		TMR clock 100MHz	45.92	uA
SIO		SIO clock 100MHz	131.5	uA
FLASH		HCLK clock 100MHz	184.5	uA
XO		HCLK is from 100MHz PLL, which takes RCO0 as input	177.4	uA
RCO		HCLK is from 100MHz PLL, which takes XO as input	77.21	uA
PLL		RCO0 as HCLK source, f_{PLL} = 100 MHz	206.5	uA

[1] For peripherals with multiple instances, the current quoted is for single modules. For example, the 4.10 mA value quoted for PGA is for one PGA module. So the total 3 PGA module current is 12.30mA.

[2] Typical values are measured at T_A = 25 °C, V_{DDG} = 15 V, V_{DD} = 3.3 V

[3] ADC analog current contain ADC analog module, bandgap and ADC reference buffer.

[4] The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

5.6 Internal 1.2V regulator characteristics

Table 5-8: Internal 1.2V regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply	-	2.97	3.3	3.63	V
VCAP12	Output voltage	Load current = 50mA	1.18	1.20	1.22	V
ΔVCAP12	Load regulation	VCAP12(50mA load) – VCAP12(200mA load)	-	-	30	mV

Figure 5-4: Internal 1.2V regulator load regulation (TA = 25 °C)

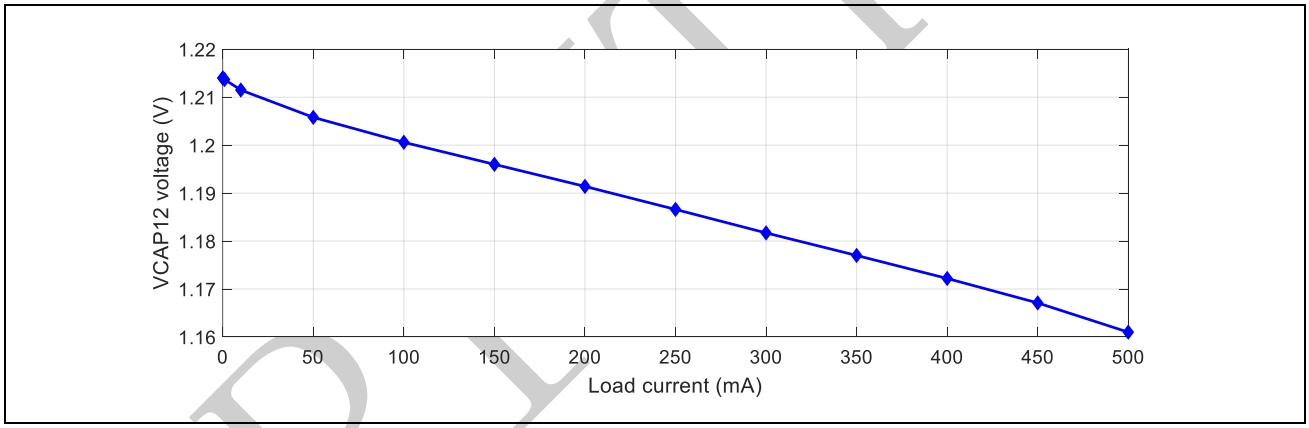
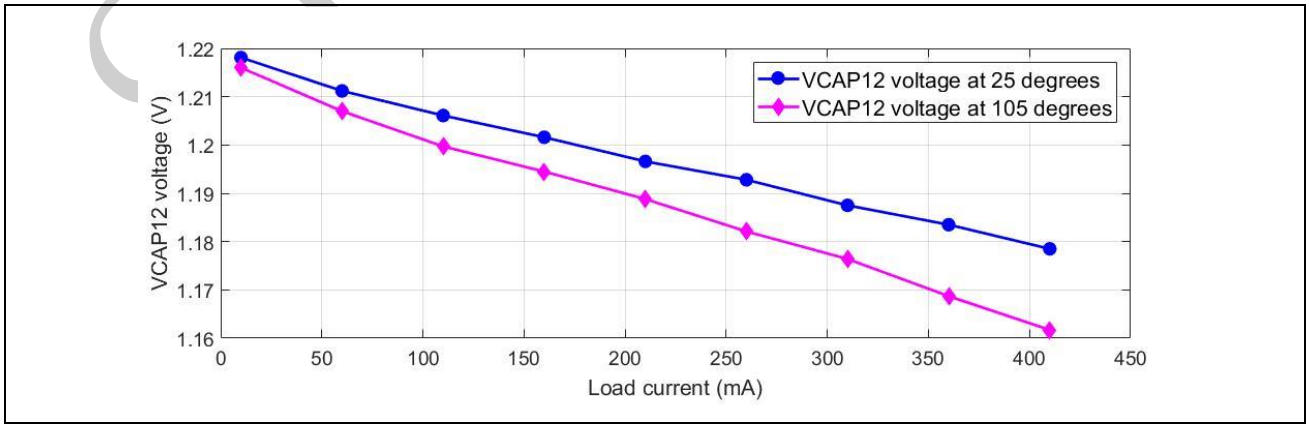


Figure 5-5: Internal 1.2V regulator load regulation with different temperature



5.7 BOD characteristics

Table 5-9: BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{DD33H_Asset}	VDD33 too high assert threshold	-	-	3.42	-	V
$V_{DD33H\_Deasset}$	VDD33 too high de-assert threshold	-	-	3.31	-	V
V_{DD33L_Asset}	VDD33 too low assert threshold		-	2.58	-	V
$V_{DD33L\_Deasset}$	VDD33 too low de-assert threshold		-	2.65	-	V
V_{DD12H_Asset}	VDD12 too high assert threshold		-	1.33	-	V
$V_{DD12H\_Deasset}$	VDD12 too high de-assert threshold		-	1.31	-	V
V_{DD12L_Asset}	VDD12 too low assert threshold(1)		-	0.94	-	V
$V_{DD12L\_Deasset}$	VDD12 too low de-assert threshold(1)		-	0.97	-	V

[1] The characteristics of VDD12 too low 0 and VDD12 too low 1 are the same.

5.8 RCO characteristics

Table 5-10: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{RCO}	RCO frequency at room temperature	T_J = 25 °C	31.936	32.00	32.064	MHz
ACC_{RCO}	RCO frequency accuracy (RCO frequency variation versus temperature)	T_J = -40~125 °C	-1	-	1	%

5.9 PLL characteristics

Table 5-11: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V

F_{VCO}	VCO frequency	-	400	500	600	MHz
F_{pfd}	Phase-Frequency Detector (PFD) input frequency	-	4	-	8	MHz
t_{LOCK}	Locking time		-	-	15	us

5.10 XO characteristics

Table 5-12: XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
F_{XO}	XO frequency	-	1	-	66	MHz

The negative resistance of the on-chip crystal oscillator at different temperature is shown in Figure 5-6~Figure 5-9. The loading capacitor CL_eff is defined as equivalent capacitance seen by the on-chip crystal.

Figure 5-6: The negative resistanQce of the on-chip crystal oscillator at 50℃

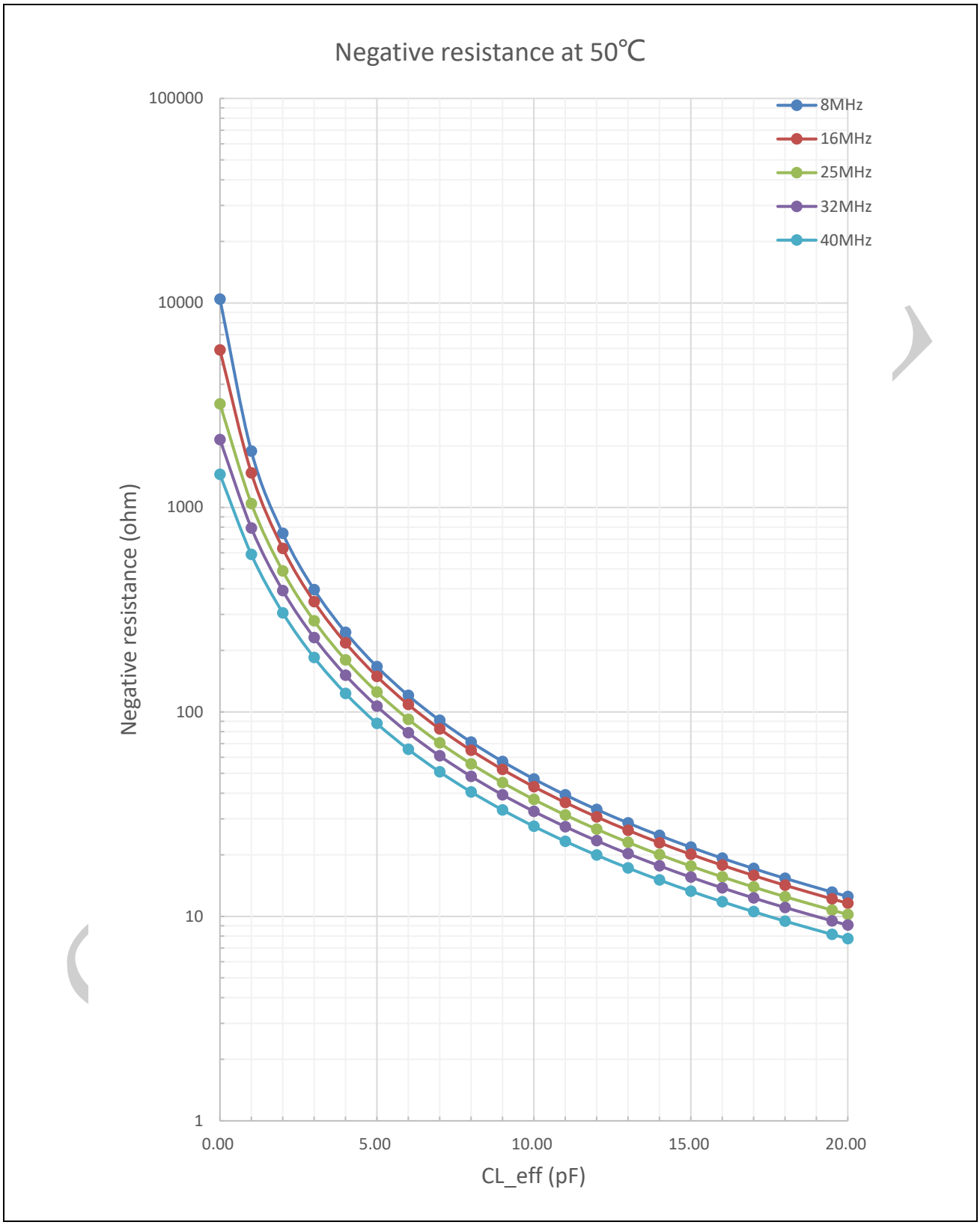


Figure 5-7: The negative resistance of the on-chip crystal oscillator at 85℃

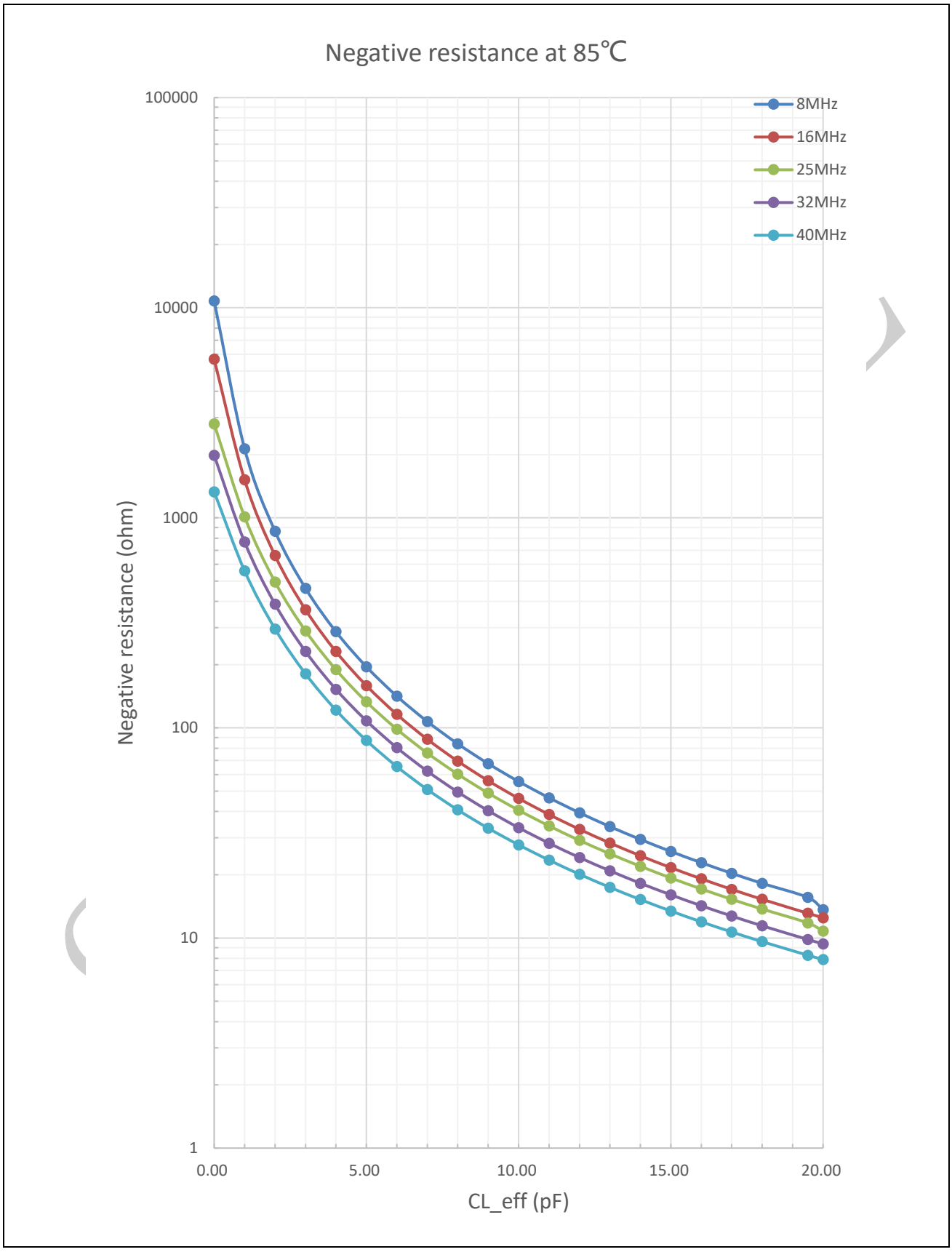


Figure 5-8: The negative resistance of the on-chip crystal oscillator at 100℃

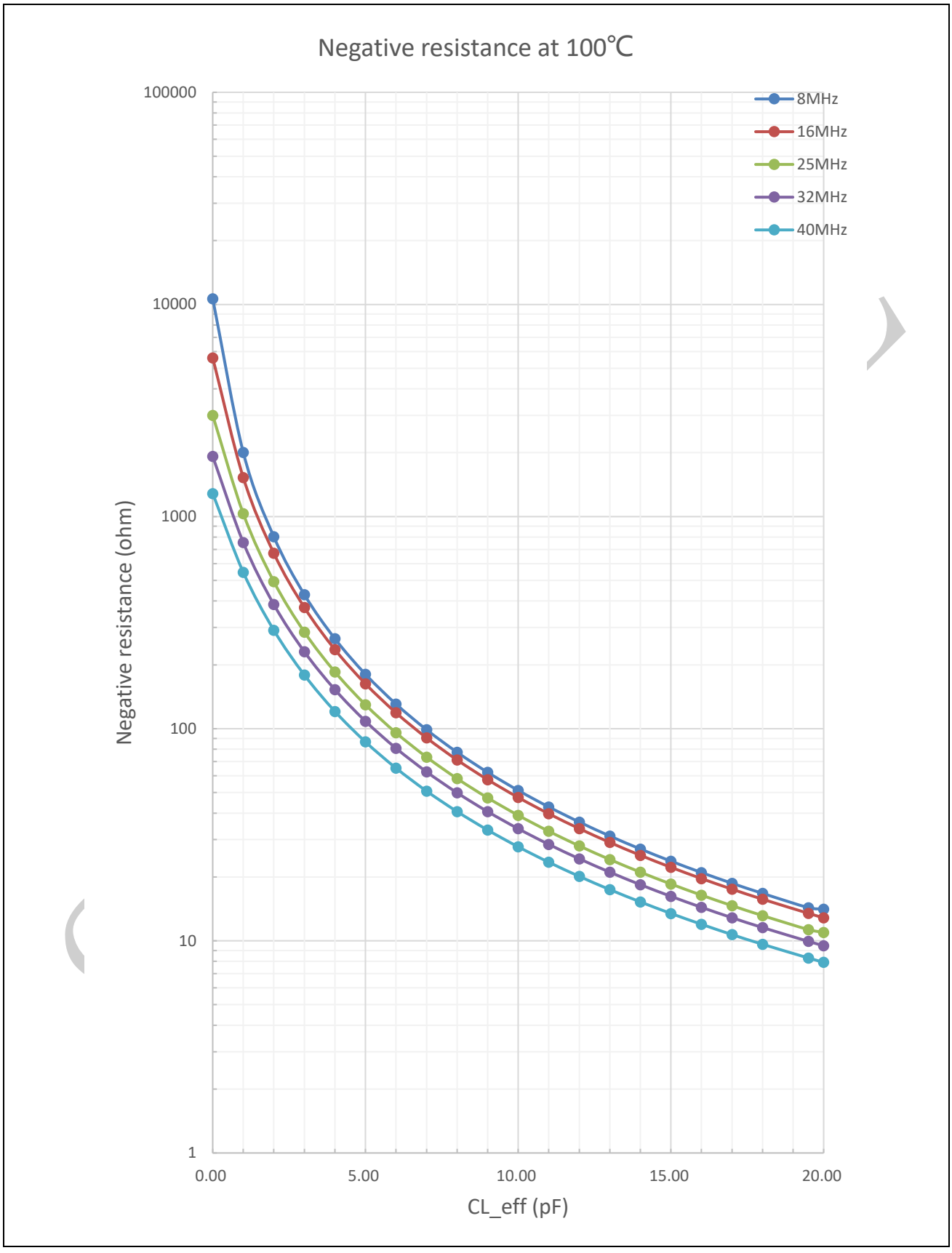
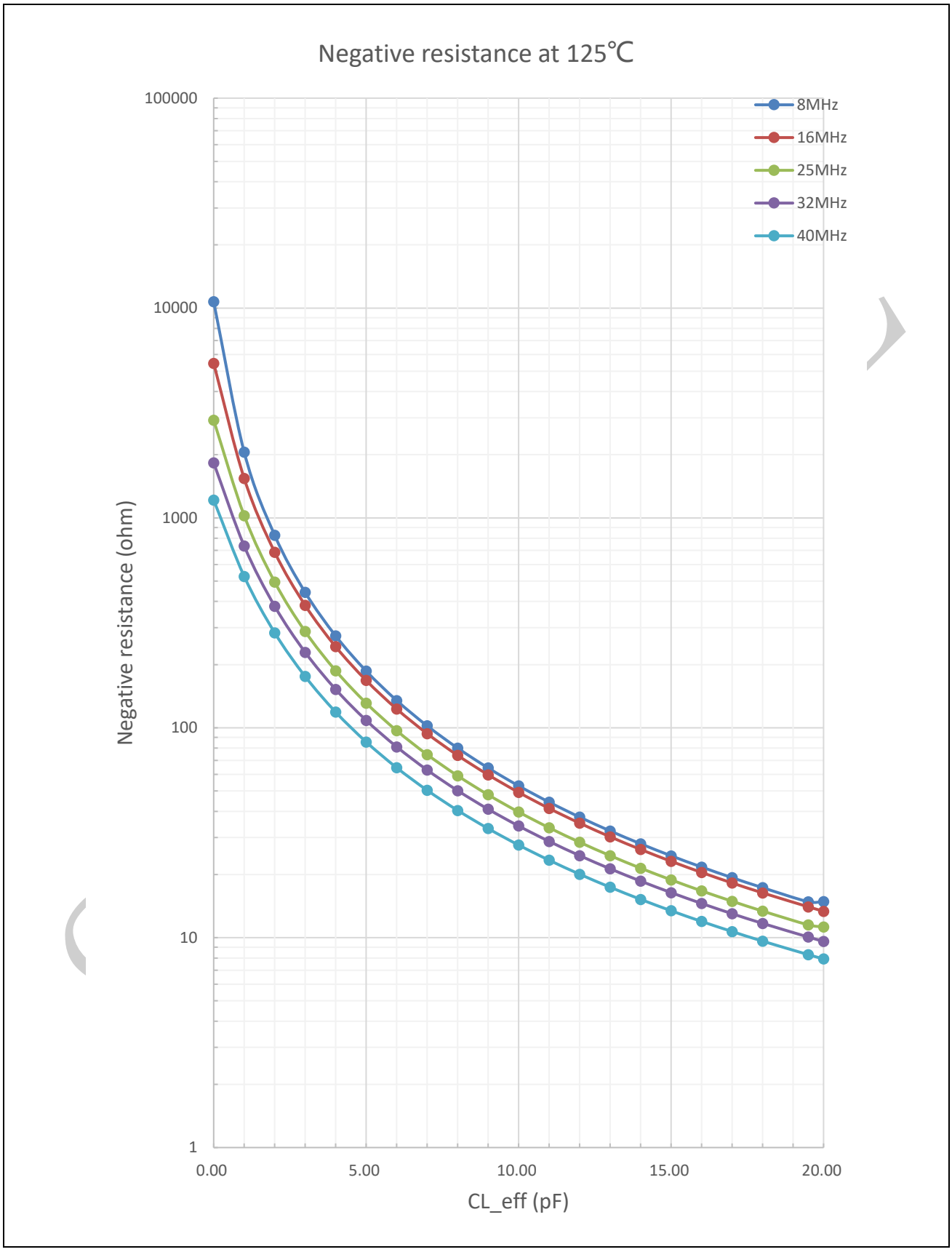


Figure 5-9: The negative resistance of the on-chip crystal oscillator at 125℃



5.11 14-bit ADC characteristics

Table 5-13: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	14	-	-	bit
F_S	Conversion speed(1)	-	-	-	4	MSPS
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{REF}	Reference voltage	-	1.194	1.2	1.206	V
I_{PAD}	Operational current	V_{DDA} = 3.3 V	-	17.1	21	mA
INL	Integral linearity error	-	-3.0	-	3.0	LSB
DNL	Differential linearity	-	-1.0	-	1.0	LSB
E_{OFF}	Offset error(2)	With calibration	-2	-	2	LSB
E_{GAIN}	Gain error(2)	With calibration	-4	-	4	LSB
E_{OFF2}	Channel to channel offset	-	-3	-	3	LSB
E_{GAIN2}	Channel to channel gain error	-	-5	-	5	LSB
T_{COEF}	ADC temperature coefficient with internal reference	-	-	26	-	ppm/°C
t_{PWRUP}	Power-up time	-	-	-	200	us
$ENOB_{DC}$	DC Noise Floor	-	-	12.0	-	bits
SNR	Signal-to-noise ratio	Fin = 100kHz, Amp = 0.94F_S, N = 8192	-	75.5	-	dB
THD	Total harmonic distortion		-	-85.0	-	dB
ENOB	Effective number of bits		-	12.2	-	bits
SFDR	Spurious free dynamic range		-	86.0	-	dB
T_{SLOPE}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	-	-	1.904(3)	-	°C/LSB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{OFFSET}	ADC output at 25 °C of the temperature sensor	-	-	162.138	-	LSB

[1] Sampling time = 110ns, conversion time = 140ns

[2] Offset and gain can be calibrated automatically by hardware.

[3] Can be reduced to 0.24 °C/LSB by PGA.

5.12 PGA characteristics

Table 5-14: PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{OUT}	Output voltage range	-	0.3	-	V_{DDA}-0.3	V
R_{IN}	Input impedance	-	-	10	-	MΩ
G	Gain	Single-ended mode	1, 2, 4, 8, 12, 16, 24, 32			-
		Differential mode	2, 4, 8, 16, 24, 32, 48, 64			-
E_{GAIN}	Gain error	Differential Gain = 2	-0.5	-	0.5	%
		Differential Gain = 64	-3	-	3	%
V_{OS}	Offset	-	-5	-	5	mV
T_{OFFSET}	Offset temperature drift	-	-	5	-	uV/ °C
SR	Slew rate	Single mode and Loading is ADC sampling capacitor	-	20	-	V/us
		Differential mode and Loading is ADC sampling capacitor	-	40	-	V/us
GBW	Gain band width	Single gain = 1	-	40	-	MHz
		Single gain = 8	-	6.8	-	MHz
		Single gain = 32	-	1.7	-	MHz
		Differential gain = 2	-	20	-	MHz
		Differential gain = 16	-	3.4	-	MHz
		Differential gain = 64	-	0.8	-	MHz
t_{SETTLE}	Settle time	Differential gain = 2	-	170(1)	220	ns
		Differential gain = 16		400	600	ns
		Differential gain = 64	-	1600	2200	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	Differential gain = 2 Fin = 10kHz, Amp = 0.94F_S, N = 8192	-	74.0	-	dB
THD	Total harmonic distortion		-	-78.0	-	dB
ENOB	Effective number of bits		-	11.6	-	bit
SFDR	Spurious free dynamic range		-	82.0	-	dB
SNR	Signal-to-noise ratio	Differential gain = 64 Fin = 10kHz, Amp = 0.94F_S, N = 8192	-	58.0	-	dB
THD	Total harmonic distortion		-	-80.0	-	dB
ENOB	Effective number of bits		-	9.4	-	bit
SFDR	Spurious free dynamic range		-	63.0	-	dB
I	Current consumption	Only one PGA	-	4.16	5.20	mA

[1] Settle time is measured by step input, and differential output change from -2.7V to 2.7V (VDDA=3.3V), the time for output to be settled with 1LSB (446uV), guarantee by design.

5.13 Analog comparator characteristics

Table 5-15: Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage (Hysteresis voltage=0)	Common mode input voltage = 1.65V	-10	-	10	mV
V_{HYST}	Hysteresis voltage(12mV)	-	-	13	-	mV
	Hysteresis voltage(24mV)	-	-	26	-	mV
	Hysteresis voltage(36mV)	-	-	42	-	mV
t_D	Delay time – comparator response time to PWM shunt down (Asynchronous)	-	-	50	-	ns

5.14 Internal 10-bit DAC characteristics

Table 5-16: DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N	resolution	Monotonic	10	-	-	bit
V_{FS}	Full scale value	-	0	-	V_{DDA}	V
DNL	Differential linearity	-	-0.5	-	0.5	LSB
INL	Integral linearity	-	-1	-	1	LSB
E_{OFF}	Offset error	-	-	5	-	mV
t_{SETTLE}	DAC settling time	Design guarantee	-	-	1	us

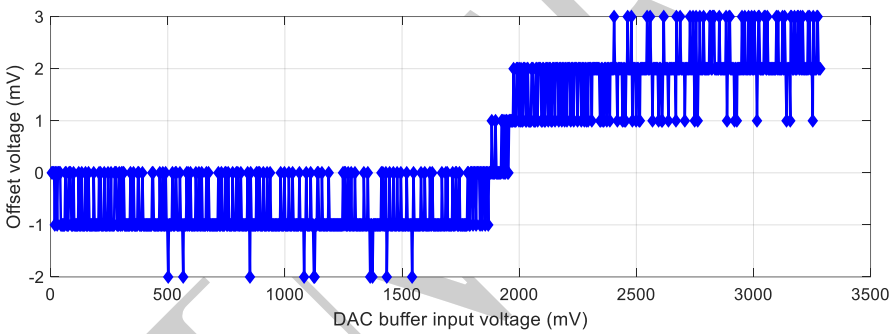
[1] The DAC is used to generate a static voltage as a threshold for the comparator and does not guarantee the performance of the waveform produced by dynamically changing the code value.

5.15 DAC buffer characteristics

Table 5-17: DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OUT}	Output voltage range	-	0.3	-	V_{DDA}-0.3	V
t_{SETTLE}	Settling time	Design guarantee	-	1	-	us
E_{OFF}	Offset error	-	-	3	-	mV
C_L	Capacitor load	-	-	-	50	pF
R_L	Resistor load	-	1	-	-	Ω

Figure 5-10: DAC buffer offset over Input voltage



5.16 Flash memory characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 5-18: Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RD}	Read access time	-	40	-	ns
t_{PROG}	Word (32-bit) program time	-	8	10	us
t_{SE}	Sector erase time	-	0.8	4	ms
t_{CE}	Chip erase time	-	8	10	ms
N_{END}	Endurance (erase/program cycle)	T_J = 85 °C	100000	-	cycles
t_{RET}	Data retention duration	T_J = 85 °C	10	-	years

5.17 Electrical sensitivity characteristics

Table 5-19: ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	Ambient temperature T_A = 25 °C		200	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	-	500	V
			Corner Pin	750	V

Table 5-20: Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 85 °C V_{DD} = 3.63V, VCAP12 = 1.32V	100	mA

5.18 Moisture sensitivity characteristics

Table 5-21: Moisture sensitivity characteristic

Symbol	Parameter	Conditions	Level	Unit
MSL	Moisture sensitivity level	-	Level 3	-

5.19 Thermal resistance characteristics

Table 5-22: Thermal resistance characteristics (LQFP48 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	-	16.84	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	72.15	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer =	52.37	°C/W

Symbol	Parameter	Conditions	Typ	Unit
		100%, Bottom layer = 5%)		

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

Table 5-23: Thermal resistance characteristics (LQFP32 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	-	18.14	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	73.59	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	53.87	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

Table 5-24: Thermal resistance characteristics (QFN32 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	-	14.33	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	67.60	°C/W
		4-layer PCB PCB Copper content (Top layer 20%, Second/Third layer = 100%, Bottom layer = 5%)	41.27	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

5.20 SPI characteristics

Table 5-25: SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	-	-	-	50	MHz
$t_{SCLK(H)}$	SCLK clock high time	-	10	-	-	ns

$t_{SCLK(L)}$	SCLK clock low time	-	10	-	-	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(MO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(MI)}$	Data input setup time	-	6	-	-	ns
$t_{H(MI)}$	Data input hold time	-	2	-	-	ns
SPI slave mode						
$t_{SU(SFRM)}$	SFRM enable setup time	-	5.6	-	-	ns
$t_{H(SFRM)}$	SFRM enable hold time	-	1.5	-	-	ns
$t_{A(SO)}$	Data output access time	-	4	-	10	ns
$t_{DIS(SO)}$	Data output disable time	-	4	-	10	ns
$t_{V(SO)}$	Data output valid time	-	-	-	9.5	ns
$t_{H(SO)}$	Data output hold time	-	3.9	-	-	ns
$t_{SU(SI)}$	Data input setup time	-	6	-	-	ns
$t_{H(SI)}$	Data input hold time	-	2	-	-	ns

6 PCB layout guidanc

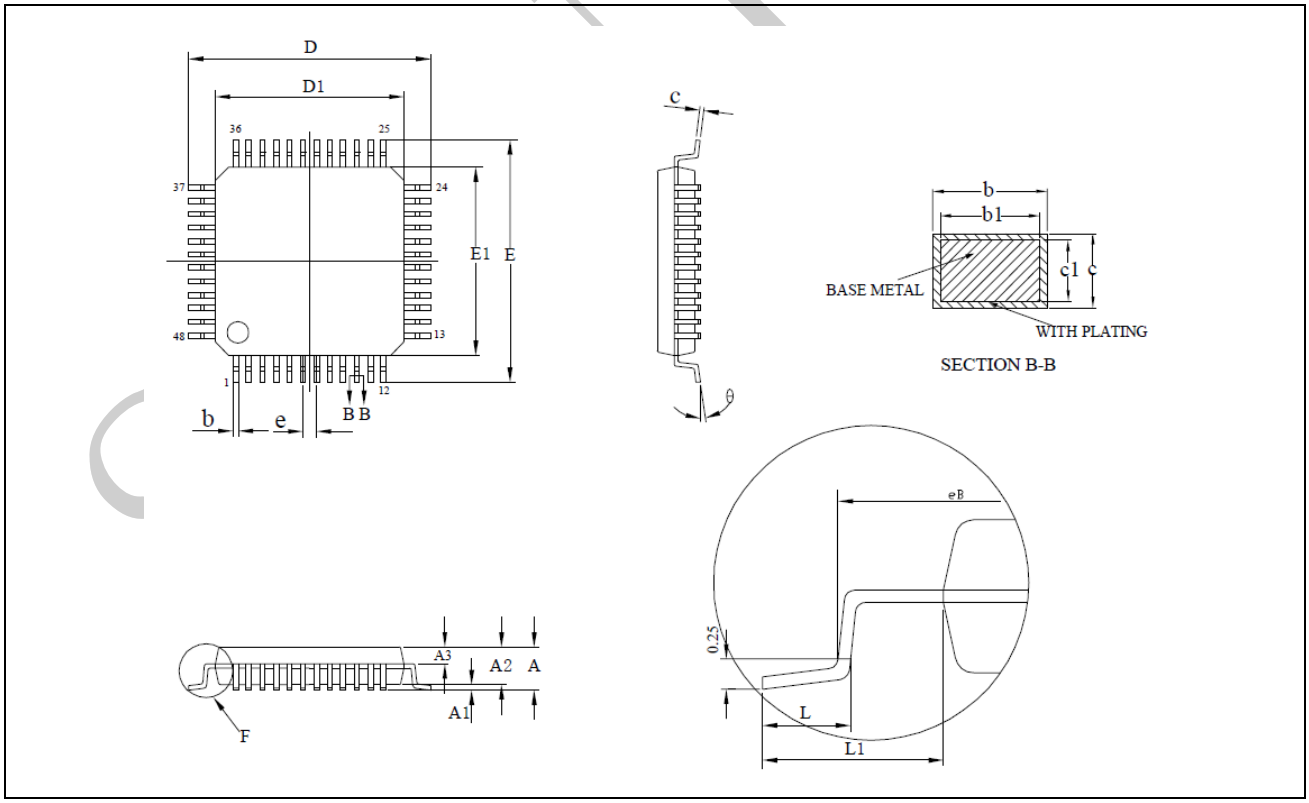
- DVDD is the feedback of buck DCDC, in order to keep the stable operation of control loop, it is recommended to keep DVDD trace away from high voltage switching trace and noisy source, such as inductor, etc.
- Keep the switching trace as short and wide as practical in order to minimize radiated emissions.
- The GND trace between the DVDD capacitor and the GND pin should be as wide as possible so that trace impedance is minimized.

7 Package information

The package type of SPC1158 is 48-pin LQFP or 32-pin QFN. The detail information is as below.

7.1 LQFP48

Figure 7-1: LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package outline



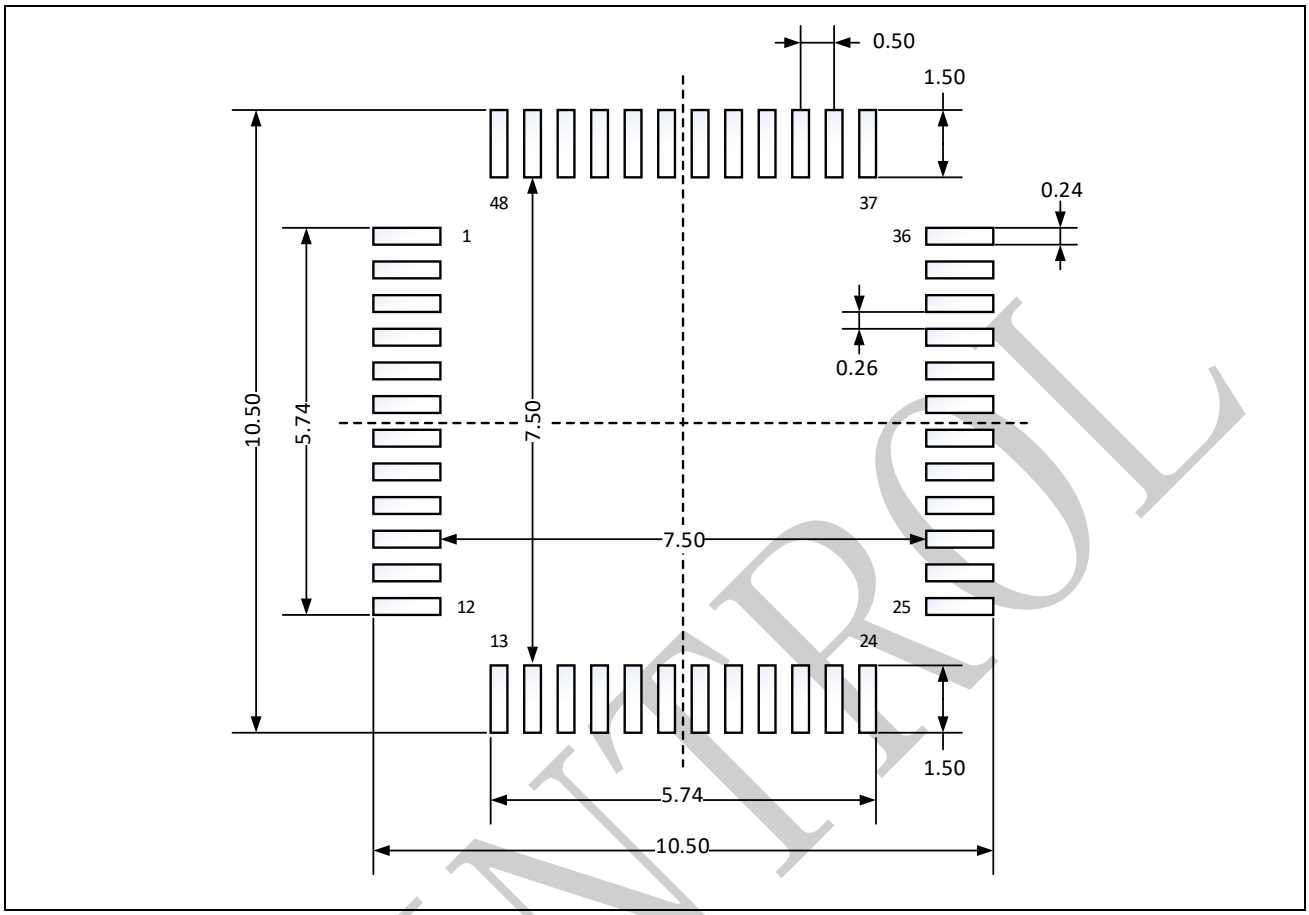
[1] Drawing is not to scale.

Table 7-1: LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
A3	0.59	0.64	0.69	0.0232	0.0252	0.0272
b	0.18	-	0.26	0.0071	-	0.0102
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.13	-	0.17	0.0051	-	0.0067
c1	0.12	0.13	0.14	0.0047	0.0051	0.0055
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
eB	8.10	-	8.25	0.3189	-	0.3248
e	-	0.5	-	-	0.0197	-
L	0.4	-	0.75	0.0157	-	0.0295
L1	-	1.00	-	-	0.0394	-
θ	0	-	7°	0	-	7°

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

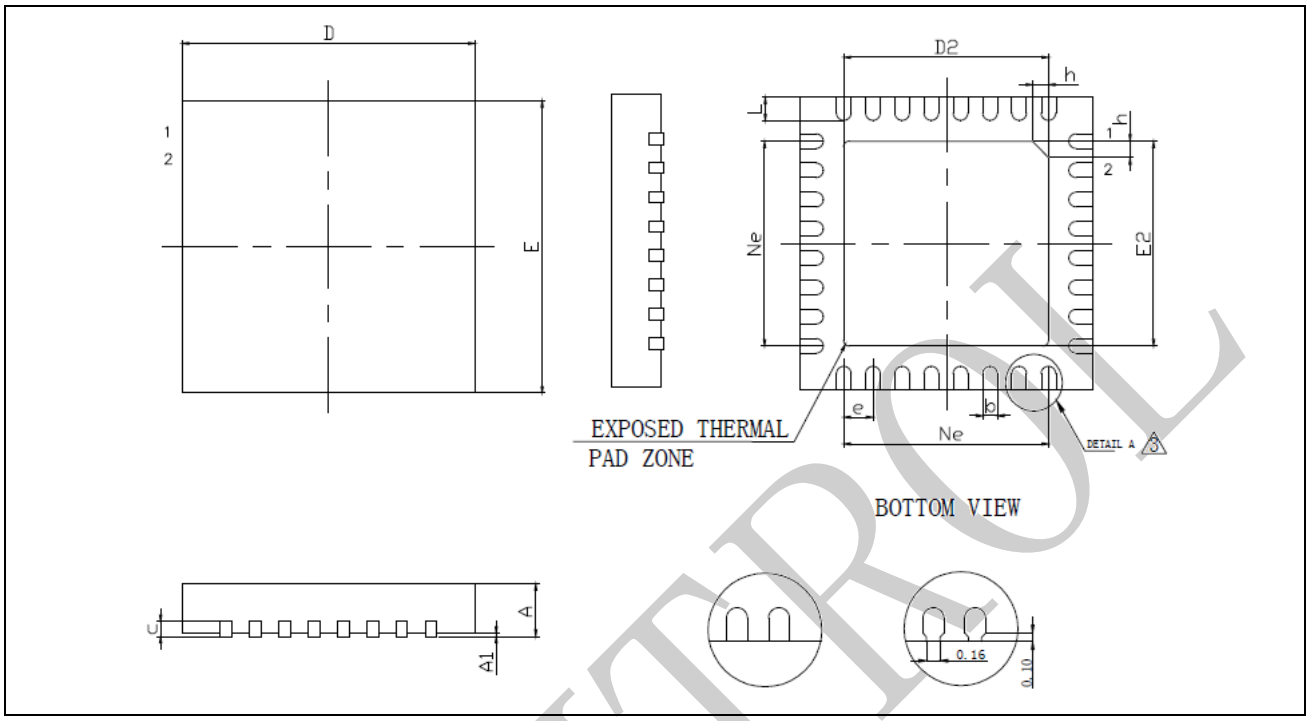
Figure 7-2: LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package recommended footprint



[1] Dimensions are expressed in millimeters.

7.2 QFN32

Figure 7-3: QFN32 – 32 pin, 5 x 5 mm quad flat no-lead package outline



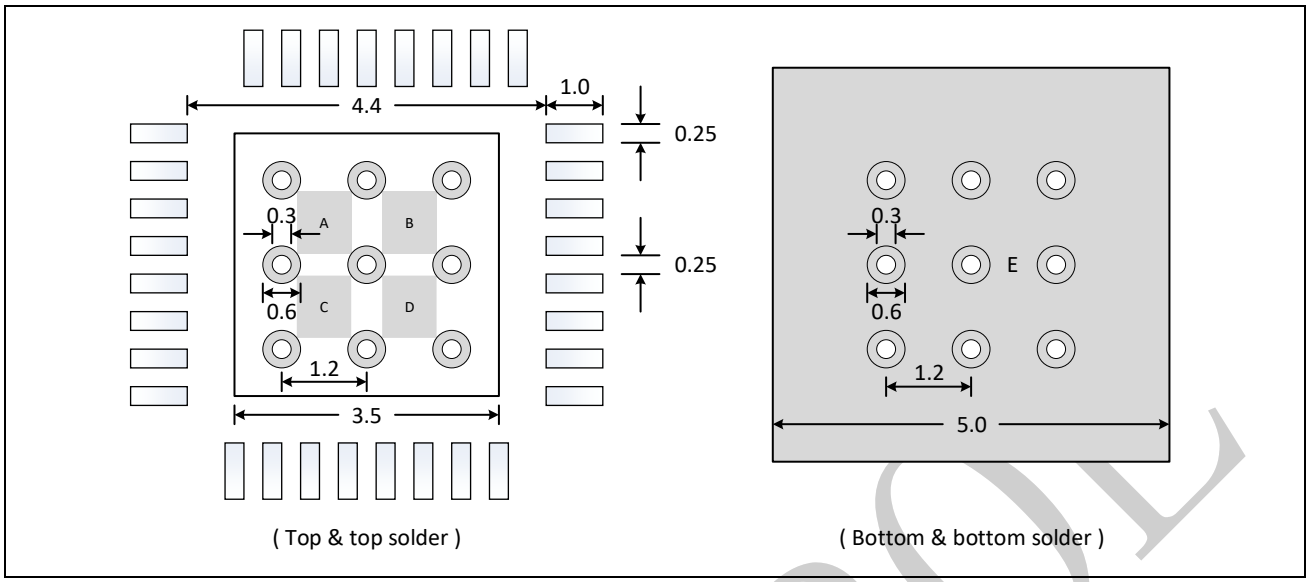
[1] Drawing is not to scale.

Table 7-2: QFN32 – 32 pin, 5 x 5 mm quad flat no-lead package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	-	0.02	0.05	-	0.0008	0.0020
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
c	0.18	0.20	0.25	0.0071	0.0079	0.0098
D	4.90	5.00	5.10	0.1929	0.1969	0.2008
D2	3.40	3.50	3.60	0.1339	0.1378	0.1417
e	-	0.50	-	-	0.0197	-
Ne	-	3.50	-	-	0.1378	-
E	4.90	5.00	5.10	0.1929	0.1969	0.2008
E2	3.40	3.50	3.60	0.1339	0.1378	0.1417
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
h	0.30	0.35	0.40	0.0118	0.0138	0.0157

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 7-4: QFN32 – 32 pin, 5 x 5 mm quad flat no-lead package recommended footprint

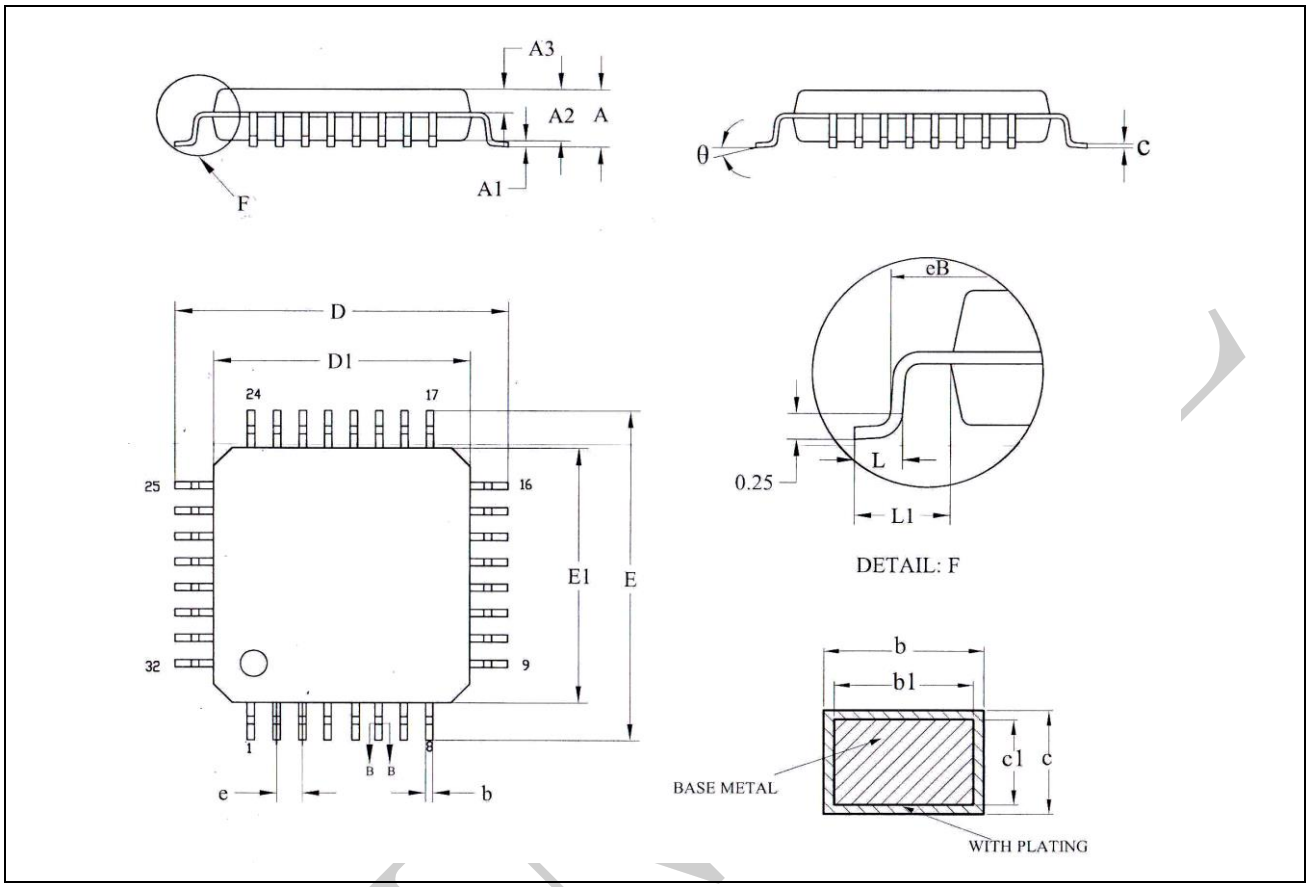


[1] Dimensions are expressed in millimeters.

[2] The A, B, C, D areas on the top layer should brush solder paste, and E area on bottom layer can either brush solder paste or not.

7.3 LQFP32

Figure 7-5: LQFP32 – 32 pin, 7 x 7 mm low-profile quad flat package outline



[1] Drawing is not to scale.

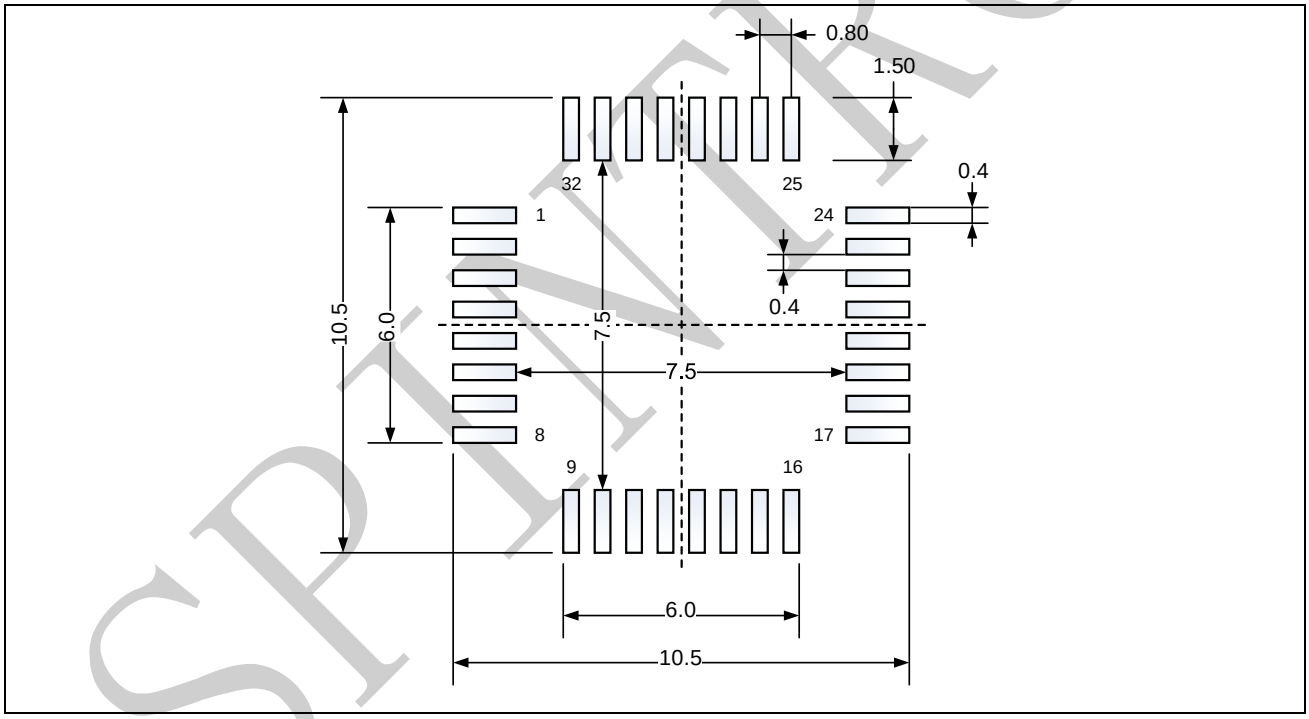
Table 7-3: LQFP32 – 32 pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
A3	0.59	0.64	0.69	0.0232	0.0252	0.0272
b	0.33	-	0.41	0.0130	-	0.0161
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.12	0.13	0.14	0.0047	0.0051	0.0055
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
eB	8.10	-	8.25	0.3189	-	0.3248
e	-	0.8	-	-	0.0315	-
L	0.45	-	0.75	0.0177	-	0.0295
L1	-	1.00	-	-	0.0394	-
θ	0°	-	7°	0°	-	7°

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 7-6: LQFP32 – 32 pin, 7 x 7 mm low-profile quad flat package recommended footprint



[1] Dimensions are expressed in millimeters.

8 Ordering information

Table 8-1: Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Package	Temperature Range	SPQ[1]	Packing
SPC1158APE48	64KB	32KB	100MHz	LQFP48	Industrial -40 °C to +125 °C	2500	Tray
SPC1158HAPE48	128KB	32KB	100MHz	LQFP48	Industrial -40 °C to +125 °C	2500	Tray
SPC1158APE32[2]	64KB	32KB	100MHz	LQFP32	Industrial -40 °C to +125 °C	2500	Tray
SPC1158HAPE32[2]	128KB	32KB	100MHz	LQFP32	Industrial -40 °C to +125 °C	2500	Tray
SPC1158API32	64KB	32KB	100MHz	QFN32	Industrial -40 °C to +125 °C	4900	Tray

[1] SPQ = Standard Pack Quantity.

[2] SIO is currently not supported in SPC1158(H)APE32.