SPD1179 DEMO Board Usage Manual

Preface

This document is intended for customers, market personnel, and developer, providing instructions on the use of the SPD1179 DEMO board and detailing the functional implementation of each hardware circuit on the board.

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Revision history

Revision	Date	Author	Status	Changes
C/0	2025-02-19	MC.Rao	Released	First release.

Terms or abbreviations

Terms or abbreviations	Description
MCU	Microcontroller Unit
UART	Universal Asynchronous Receiver/Transmitter

1 Introduction of SPD1179 Board

Name of Board: EVB_SPD1179DPW48_V2.1

MCU: SPD1179

Scenarios of application: Full-function debugging of SPD1179 chips

- The typical operating voltage of the board is 12V (recommended operating voltage 5.5V to 24V)
- Rated output current 15A (If a larger output current is required, install a heat sink)
- Integrate the LIN communication functions of LIN PHY internally
- Single/triple resistance current sampling
- Provides PWM signal setting and feedback functions
- Integrated single gain selective differential operational amplifier, 13-bit ADC, temperature sensor, and overcurrent protection comparator
- Integrated VDD5EXT LDO circuit to power external sensors
- Most pins have the ECAP function to capture input levels
- Provides the UART/LIN/SWD/SPI communication function
- Integrated current type predrive module
- Supports deep sleep function and LIN/MON pin wake-up function

2 Function description of schematic and selection reference of component

Figure 2-1: EVB_SPD1179DPW48_V2.1 Board schematic

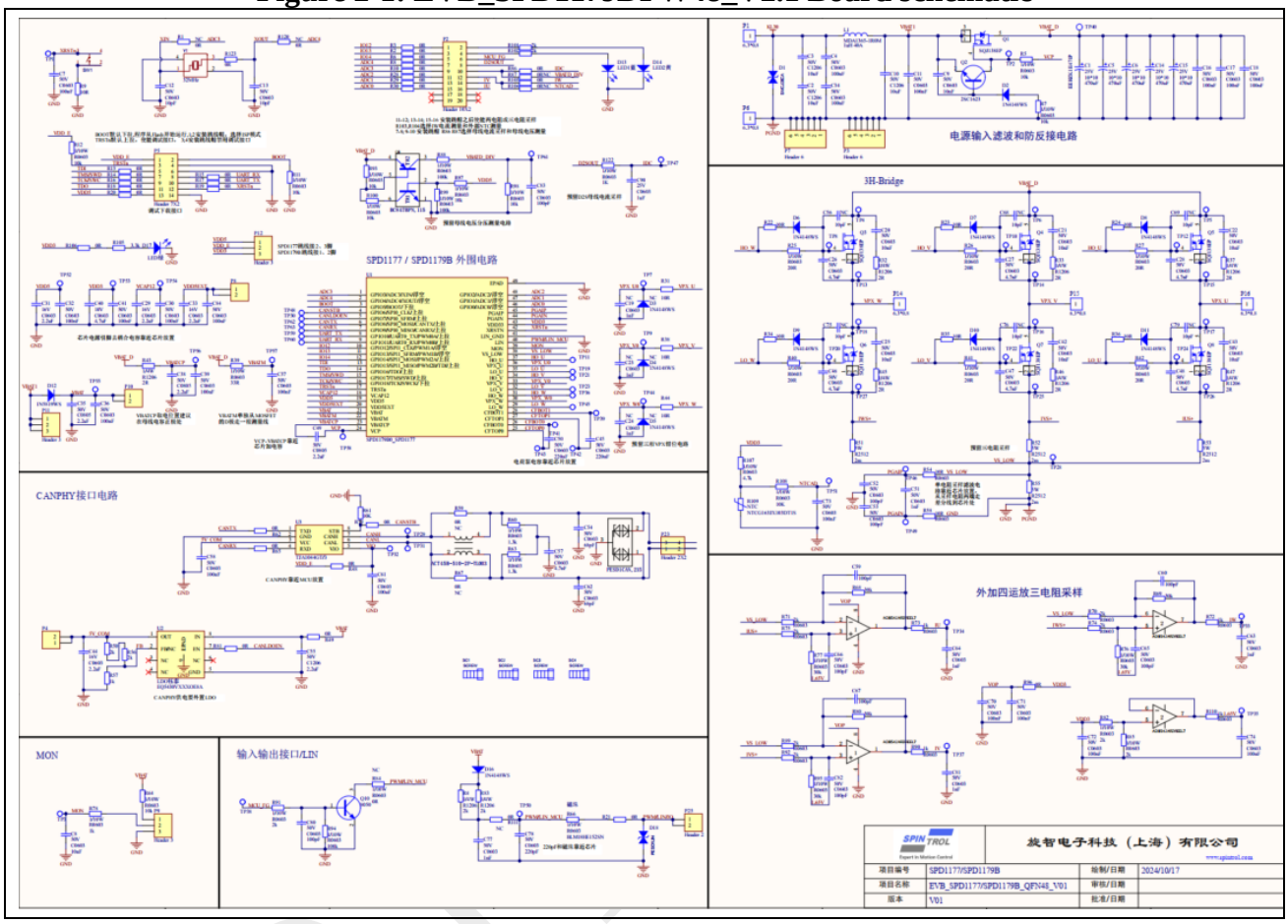
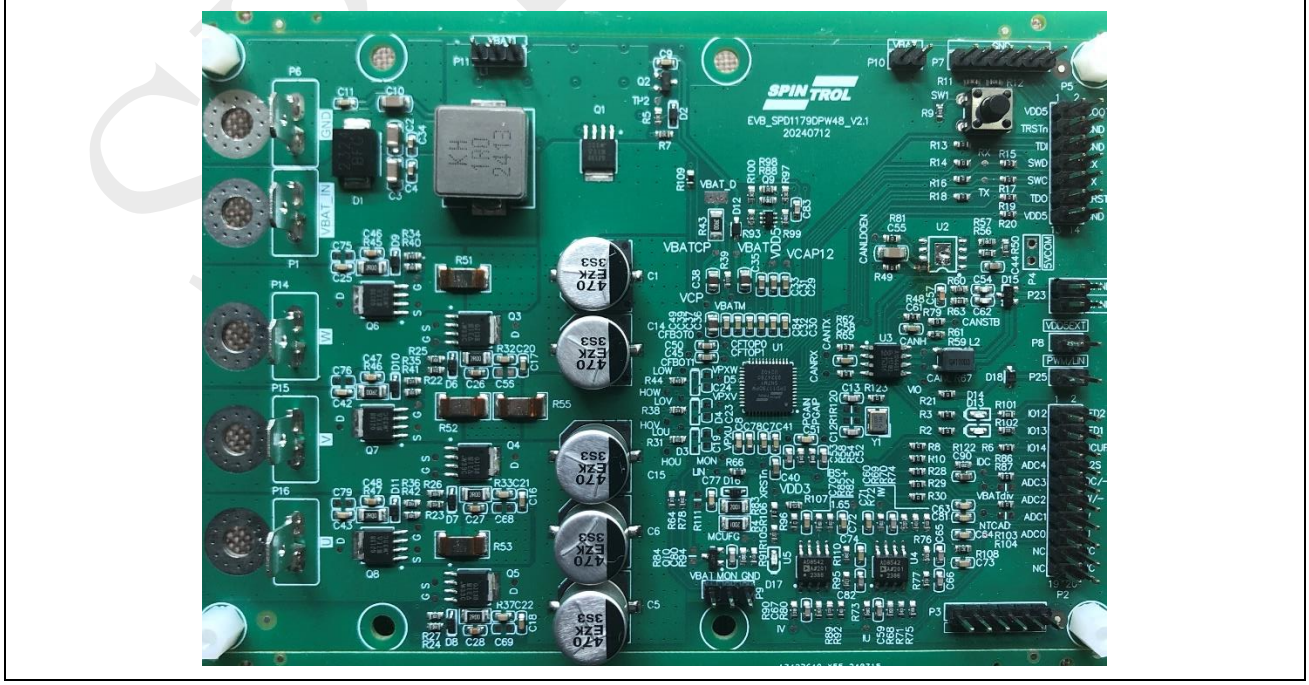


Figure 2-2: EVB_SPD1179DPW48_V2.1 Board



2.1 Settings of hardware

2.1.1 Configuring the Boot Mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM.

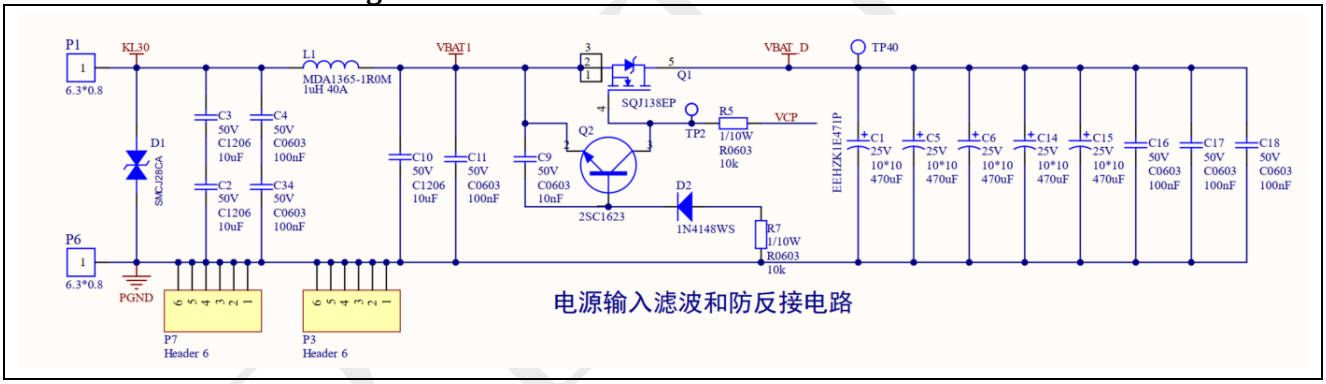
- If GPIO5(BOOT) is high upon power-on reset, XRSTn pin reset or the system reset request from the ARM® Cortex-M4F, ISP boot mode is entered. The boot loader reprograms the embedded Flash by using UART interface. When UART interface is used, GPIO10 is configured as UART0_TXD and the GPIO11 is configured as UART0_RXD.
  - For all other cases, the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000.

In hardware Settings, the default is to enter Flash boot, both TRSTn is high, GPIO5(BOOT) is low. Users can adjust the functions of the board according to their needs by means of jumpers.

2.2 Power Supply and power section

The main power supply of the board is provided by the input power supply after filtering and anti-reverse circuit, and then the voltage required for the work of the chip is generated by the integrated LDO in the chip.

Figure 2-3: Power filter and anti-reverse circuit



2.2.1 Current Sampling

There are two methods for processing the signals from the sampling resistors:

- Three-resistor sampling: After sampling the three-phase current, it is fed to the ADC pin of the chip after passing through the 1.65V op-amp bias calculation circuit.
- Single-resistor sampling: After the resistance sampling signal is processed by the internal DPGA module, an over - current protection judgment is made on it, or it is analyzed to obtain the current values of each phase.

Figure 2-4: Three-resistor sampling

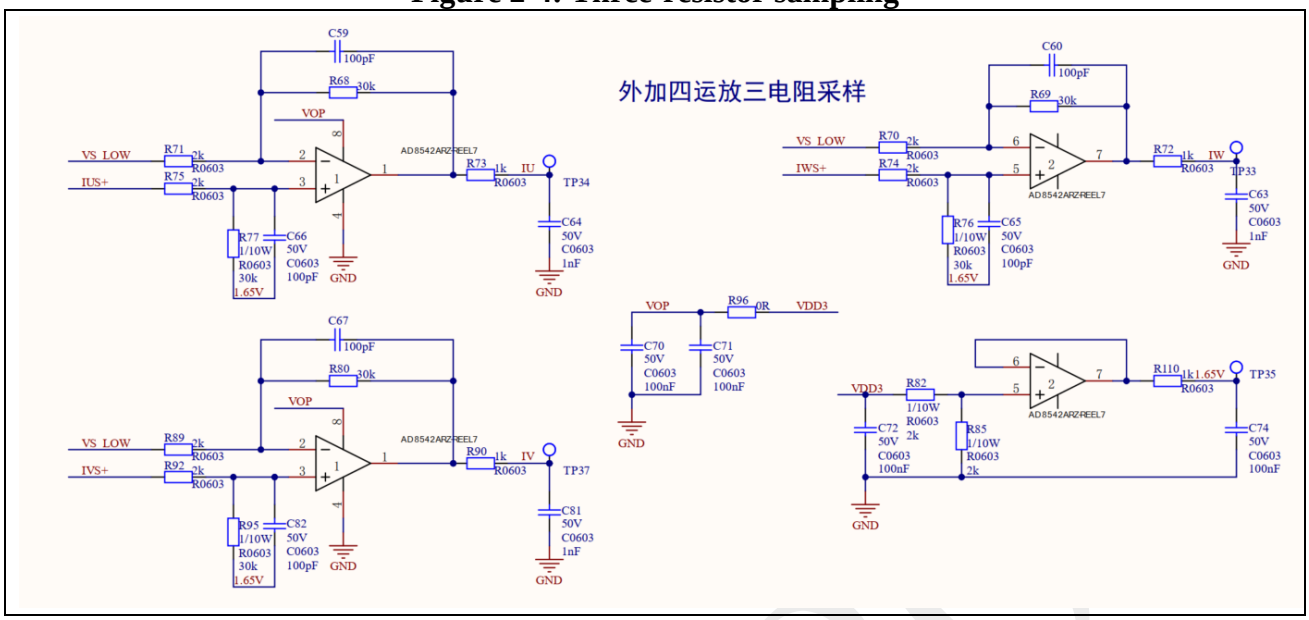
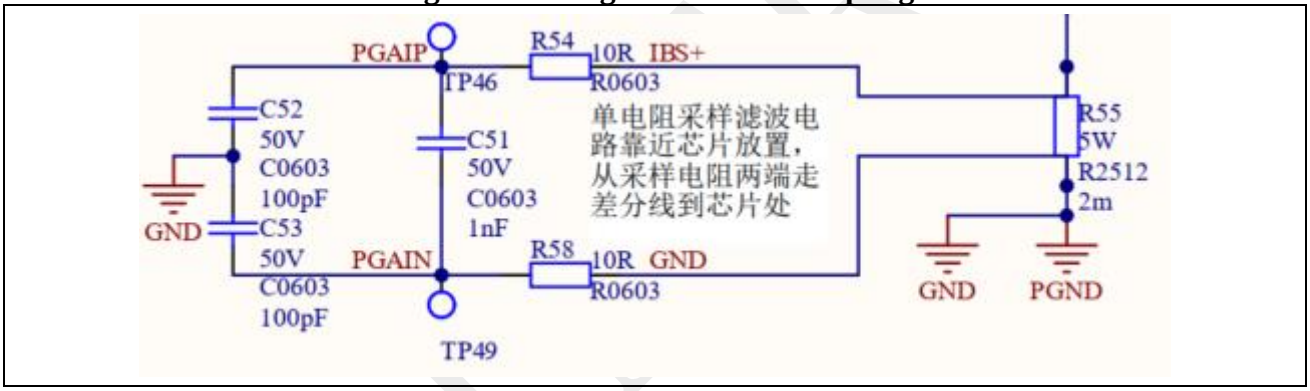


Figure 2-5: Single resistance sampling



2.2.2 Chargepump

The core of SPD1179 current-type pre-drive is a two-stage charge pump circuit, which uses two-stage charge pumps to generate VCP voltage higher than the three-phase bridge bus voltage 12V. Then, the VCP voltage is utilized to generate a controllable current source, which is used to drive and control the gate-source (GS) voltage of the three-phase bridge of MOSFETs.

The charge pump section includes two flying capacitors, CF0 and CF1, which are connected between CFTOP0 and CFTOP1, and CFBOT0 and CFBOT1, respectively. The flying capacitors have a value of 220nF(50V). The bypass capacitor C_{VCP} for the charge pump is connected between VCP and VBATCP, with a recommended value of 1uF(with a withstand voltage of over 25 V).

Table 2-1: Recommended Value Of The Decoupling Capacitor In The Power Domain Of SPD1179 Chip

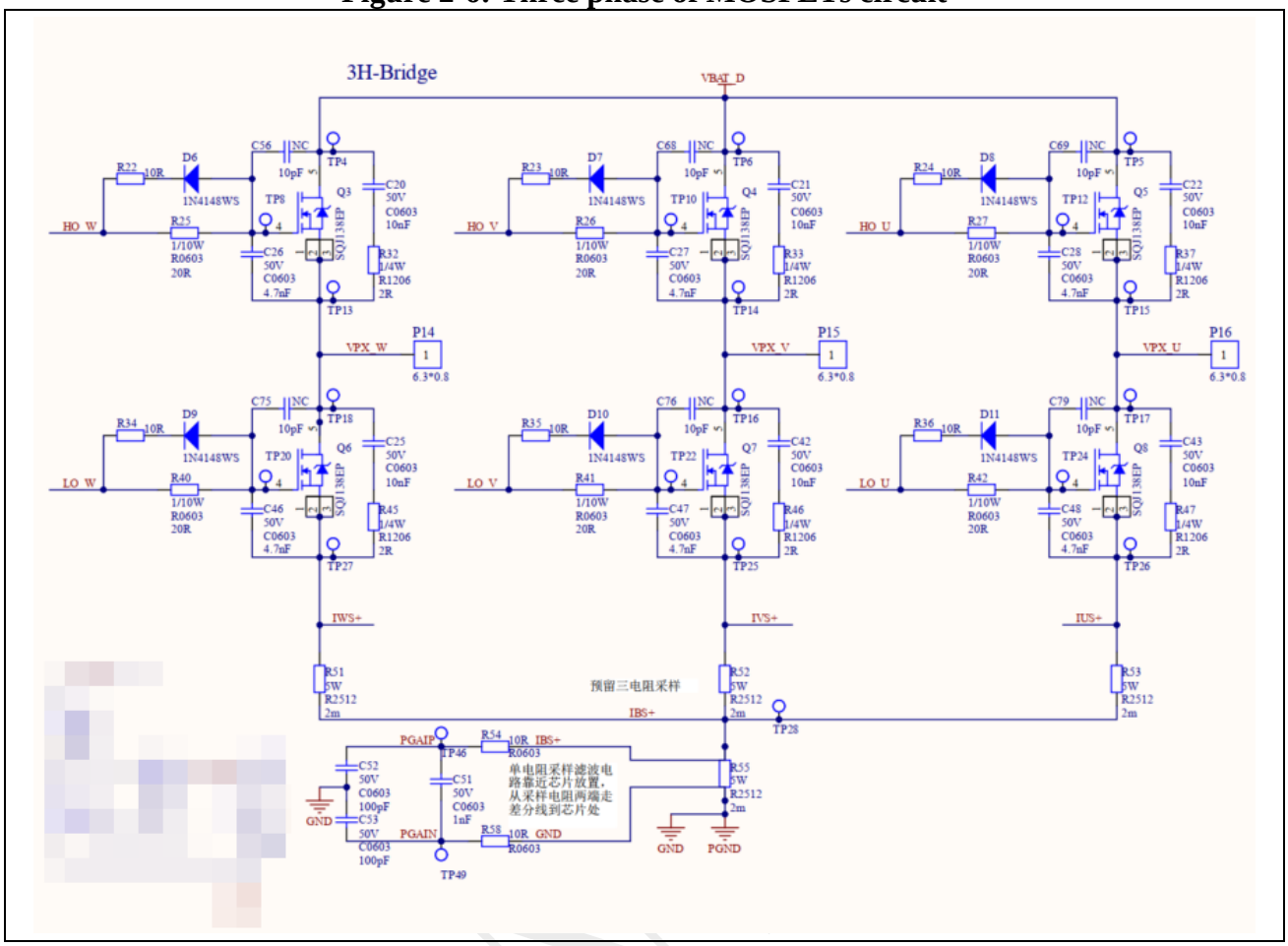
Signal name	Type	Description
VBAT	Power Source	A single power input of the chip, and the high frequency decoupling capacitors of 2.2uF+100nF (50V) are placed near the VBAT and GND pins.
DVDD5	Power Source	Digital power supply, 2.2uF+100nF high frequency decoupling capacitors should be placed near DVDD5 and GND.

DVDD33	Power Source	Analog power supply of the MCU is 3.3V, and the high-frequency decoupling capacitor of 4.7uF+100nF are placed near the DVDD33 and GND.
VCAP12	Power Source	1.2V, and a high-frequency decoupling capacitor of 2.2uF+100nF should be placed near the VCAP12 and GND.
DVDD5EXT	Power Source	5V power supply for external sensors, and a 2.2uF+100nF high frequency decoupling capacitor is placed near the DVDD5EXT and GND.
EPAD	Chip Reference Site	The GND plane of the chip. The chip also has two GND pins that need to be directly connected to the EPAD.
VBATM	Power Source	A measurement pin for the power input of the upper bridge of the three - phase bridge. Place a 100 nF (50 V) high - frequency decoupling capacitor nearby between the VBATM pin and the GND pin.
VBATCP	Power Source	The power input pin of the charge pump. Place a 2.2 μF (50V) high - frequency decoupling capacitor in close proximity between VBATCP and GND.
VCP	Power Source	The power output of the charge pump. Place a 2.2uF high - frequency decoupling capacitor (with a withstand voltage of over 25V) in close proximity between VCP and VBATCP.

2.2.3 Three-phase MOSFET bridge

The three-phase bridge is the most critical part of the power module. The pre-drive outputs HO_U/V/W of SPD1179 serve as the control signals for the gates (G) of the high-side MOSFETs in the three-phase bridge. The VPX_U/V/W signals are the source (S) signals of the high-side MOSFETs, forming the high-side drive loop. The LO_U/V/W signals control the low-side MOSFETs of the three-phase bridge. The low-side drive signals use the chip GND as the reference ground, meaning the low-side drive loop must pass through the current-sampling resistor and eventually return to the chip GND.

Figure 2-6: Three phase of MOSFETs circuit



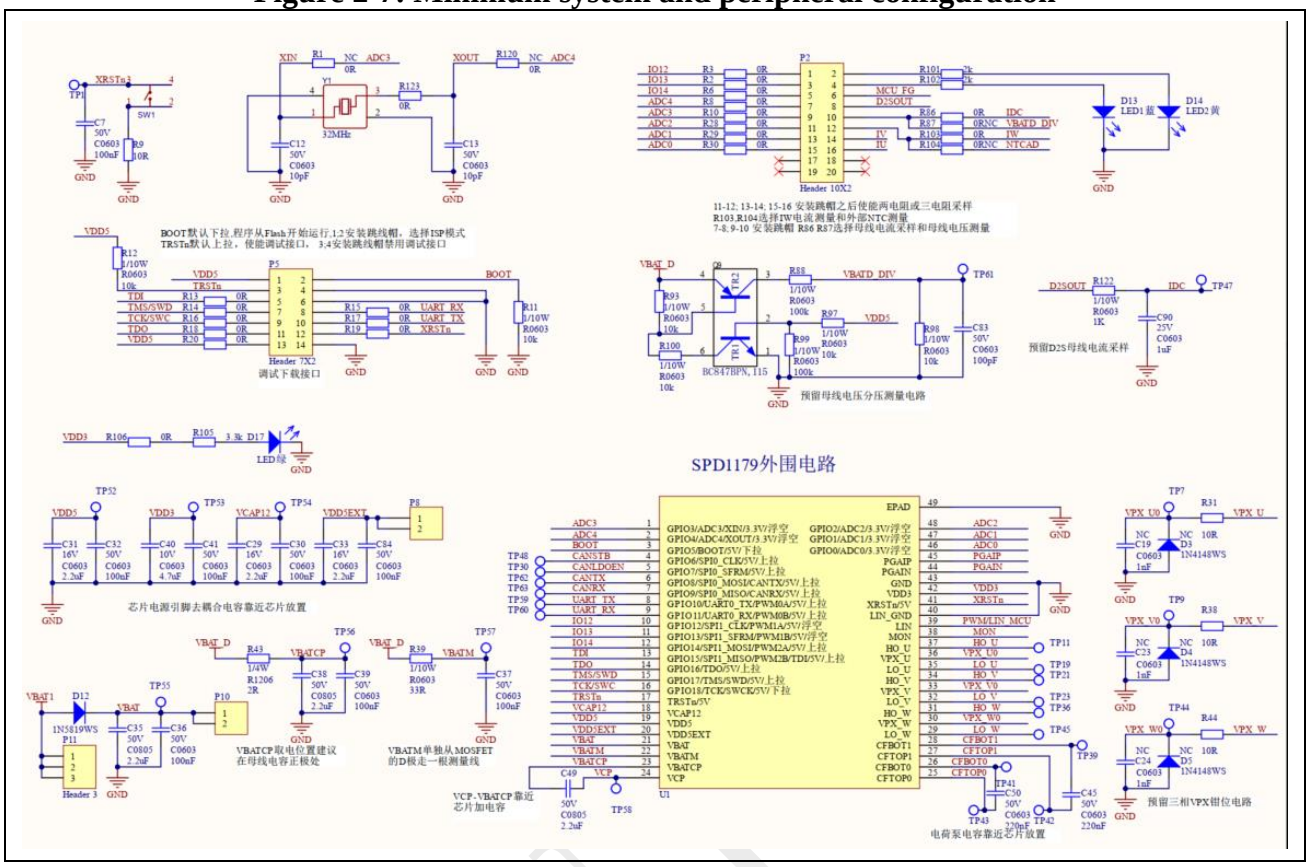
2.3 Peripheral circuit

2.3.1 Minimum system and peripheral configuration

The XRSTn pin is the global reset pin of the chip, which can reset all functional modules of the chip at low power level. If the low effective time is longer than 5 seconds, all power modules are reset and powered on again.

The SPD1179 chip has two internal RC oscillators, RCO0 is a factory-calibrated 32MHz internal RC clock (clock frequency error ±1.5% across the full temperature range) that can be used as an input to the PLL; RCO1 is a 32MHz internal RC clock, which is a backup clock for safety. XO is the clock input from external crystal oscillator or external clock source. PLL can provide up to 100MHz internal clock. For most occasions with low clock frequency requirements, the RCO0 clock inside the chip can be used directly. For applications with high real-time requirements such as CAN communication, an external crystal oscillator is required.

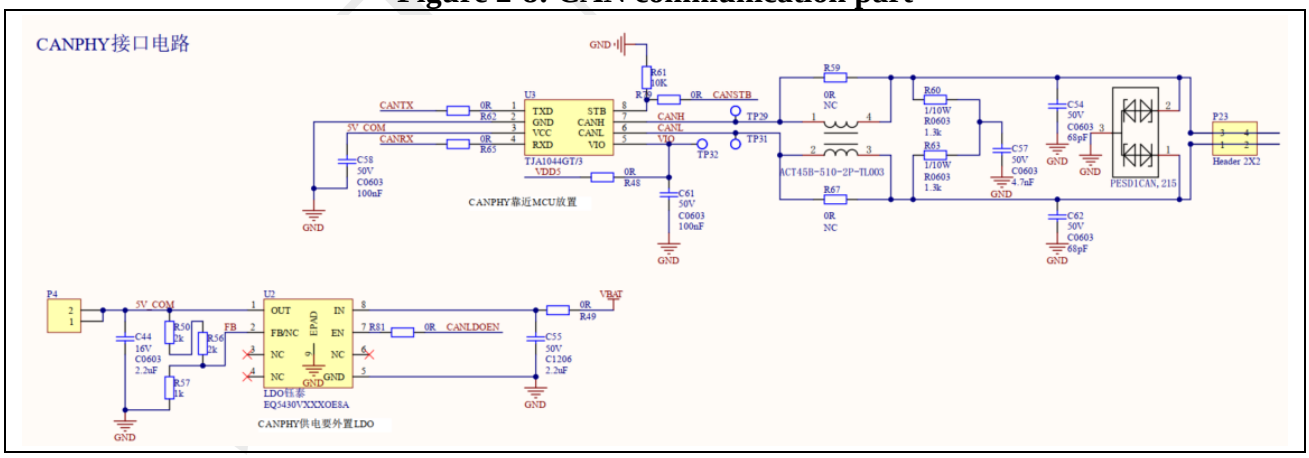
Figure 2-7: Minimum system and peripheral configuration



2.3.2 CAN communication

The SPD1179 provides one CAN module, which requires an external CAN transceiver for use.

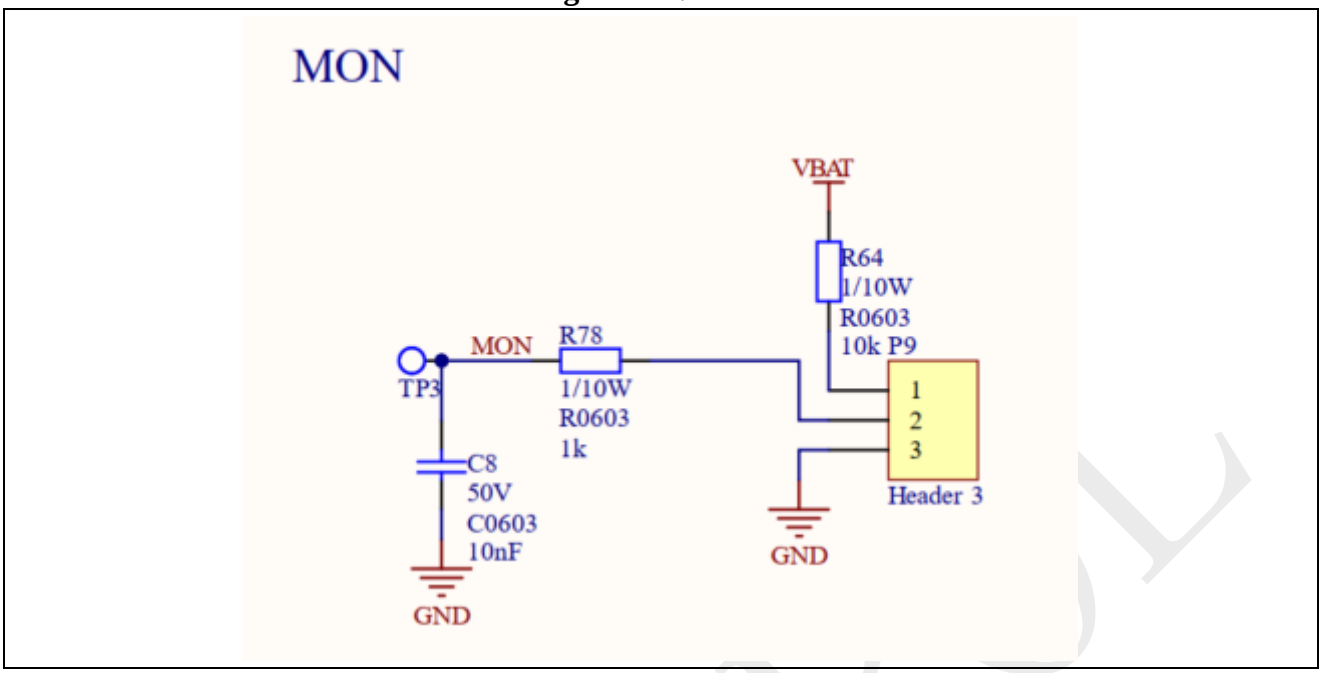
Figure 2-8: CAN communication part



2.3.3 MON

The MON pin input level can be compared with VBAT/2 inside the chip, and the logic signal after the comparison can be output to the MCU; and can also be used to wake up when the chip is in Sleep mode.

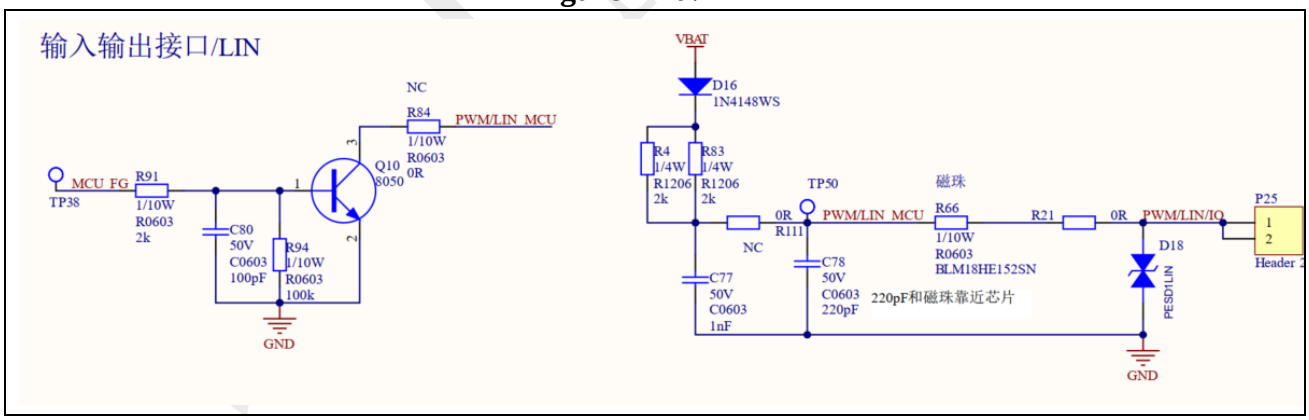
Figure 2-9：MON



2.3.4 LIN

The SPD1179 chip integrates a LIN communication module internally, which complies with LIN spec 2.2A and SAEJ2602-2 communication protocols, and the communication rate can reach up to 20kbps. During the chip program downloading, the LIN communication rate can reach up to 115.2kbps. LIN signal can be used as the wake-up source for the chip to exit from Stop and Sleep modes. Generally, when the LIN input is lower than 0.5*VBAT voltage, the chip will be woken up. The LIN transmitter is integrated with overcurrent and overtemperature protection functions, TXD timeout detection functions, and TXD slope control functions.

Figure 2-10：LIN



- If the SPD1179 is used in slave mode, connect a 220pF capacitor to the ground near the LIN pin and disconnect the R111. At the same time, the chip corresponding to the LIN pin is integrated with a VBAT pull-up diode and 30KΩ resistance, so there is no need to add an additional external 30KΩ pull-up resistance.

- When SPD1179 is used as the master mode, select an appropriate pull-up resistor and ground capacitance to ensure that the waveform slope in the LIN conformance test meets specifications. For development board hardware, R83, R4, C77, and R111 are retained as hosts, and C78 is removed.